SHT Nº	ISSUE 1	2	3	4	5	6	7
1	1	2	3	3			
2	1	1	1	1			
3	1	1	1	1			
4	1	1	1	1			
5	1	1	1	1			
6	1	1	2	3			
7	1	1	1	1			
8	1	1	1	1			
9	1	1	1	1			
10	1	1	1	1			
11	1	1	1	1			
12	1	1	1	1			
13	1	2	2	2			
14	1	2	2	2			
15	1	2	2	2			
16	1	1	1	1			
17	1	1	1	1			
18	1	1	1	1			
19	1	1	1	1			
20	1	2	2	2			
21	1	2	2	2			
22	1	2	2	2			
23	1	2	2	2			
24	1	2	2	2			
25	1	1	1	1			
26	1	1	1	2			
27	1	1	1	1			
28	-	-	1	1			
29	-	-	-	1			
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SHT Nº	ISSUE
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ISSUE	1	2	3	4
MOD Nº	1374	1505	1588	1796
DATE	26-4-66	29-6-66	26-8-66	29-11-66

1

DRAWN	DATE	APPVD	SHEET
C. CLARKE.	26-4-66.	E.K. Stoneburgh	SHEET 1 OF 29

TITLE	DRG Nº
FACING SHEET 920 B L.S.A. ELEMENT. LOGIC SYMBOLS & CIRCUIT DIAGRAMS.	322 A 7191

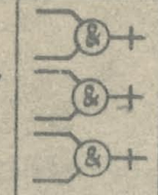
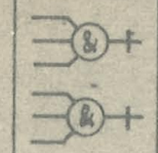
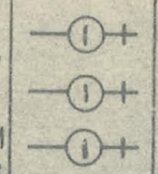
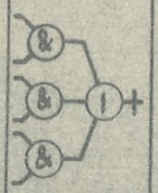
L.S.A. DESIGN NOTES.

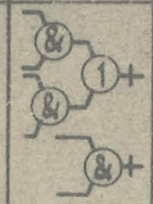
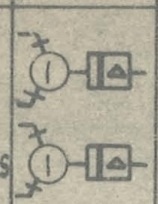
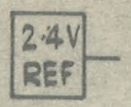
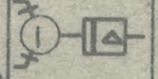
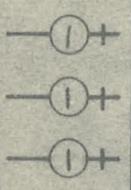
ELLIOTT BROTHERS (LONDON) LTD.

322A/191

SHEET No 2 OF

DRAWN C.A.C. ISSUE No 1
CHECKED CS 456 A.R. No 1374
APPR VED DATE 26-4-66
DATE INITIAL C.A.C.

L.S.A. No. AND NAME	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX. FAN OUT LOAD IN UNIT INPUTS			REMARKS.
			0 – 80°C	-20 – 80°C	-40 – 80°C	GENERAL: +6V RAIL — 2·2KΩ ±5% resistor. A UNIT INPUT: DIODE PURCH. 101.
01 2 INPUT NAND GATES		1·2	11	9	8	1 INPUT = 1 UNIT INPUT TYPICAL SWITCH ON TIME = 10n.s. (O/P -VE GOING) FROM + 2V TYPICAL SWITCH OFF TIME = 15n.s. (O/P + VE GOING) TO + 1·2V.
02 3 INPUT NAND GATES		1·2	11	9	8	SPEED OF +VE GOING EDGE DETERMINED BY No. OF FAN OUT, STRAY CAPACITY, CAPACITY OF BACK BIASSED DIODES & UNSELLECTED LOADS. CAPACITIVE LOADING COULD TOTAL 200 PF. AND CAUSE 50n.s. DELAY, THIS MAY BE REDUCED BY ADDING AN R TO +6V.
03 4 I/P NAND GATE PLUS 2 INVERTERS		1·2	11	9	8	BUT AVAILABLE FAN OUT IS REDUCED. E.G. PULL UP OF 2K REDUCES FAN OUT BY 1 UNIT.
04 CONTROL MATRIX WAVEFORM AMPLIFIERS		2·5	3	2	2	USED FOLLOWING A MATRIX DIODE. 1 INPUT = 0·6 UNIT INPUTS.
05		1·2	11	9	8	AS FOR L.S.A's 01, 02 AND 03.

L.S.A. No. AND NAME.	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX. FAN OUT LOAD IN UNIT INPUTS. 0-80°C	-20-80°C	-40-80°C	REMARKS
						GENERAL +6V RAIL — 2·2KΩ ± 5% — A UNIT INPUT = DIODE PURCH 101.
06		1·2	11	9	8	AS FOR LSA'S 01, 02, AND 03.
07 PULSE GENERATORS		2·4	17	16	14	Δ = 100 n.s. ± 10% 1 INPUT = 3 UNITINPUTS. USED WITH LSA 08 (2·4 V. REF. GEN) LEADS SHOULD BE KEPT SHORT TO AVOID +VE GOING O/P PULSES BEING SHORTENED. SEE NOTES ON C. LOADING IN LSA'S 01, 02 AND 03.
08 VOLTAGE REFERENCE		—	50	50	50	USED AS 2·4 V REFERENCE SUPPLIER TO PULSERS 07, 09, 13 AND 14. A PULSER INPUT FOR THIS LSA = 2·0 UNIT INPUTS.
09 PULSE GENERATOR		2·4	17	16	14	1 INPUT = 3 UNIT INPUTS. Δ = 470 n.s. ± 10% USED WITH LSA 08.
11 CABLE TRANS-MITTERS.		1·2	6	4	3	1 INPUT = 1 UNIT INPUT. USED PRECEDING LSA 12 OR LSA 17.

L.S.A. DESIGN NOTES.

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

DRAWN C.A.C.
CHECKED CS456
APPROVED [illegible] 20/5/66
DATE
INITIALS

ISSUE No. 1
A.R. No. 1374
DATE 26-4-66
INITIALS C.A.C.

INSTRUCTION SHEET 322A/7191

SHEET No. 3 OF

LSA DESIGN NOTES. 322A7191

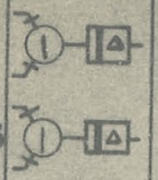
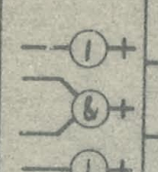
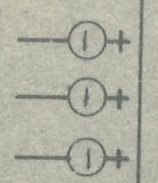
ELLIOTT BROTHERS (LONDON) LTD.

DRAWN C.A.C. 26-4-66
CHECKED CS456 10.5.66
APPROVED
DATE
INITIALS

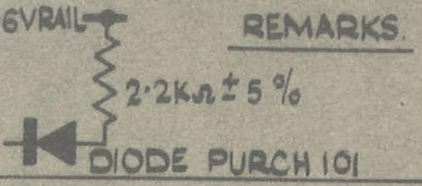
ISSUE No. 1
A.R. No. 1374
DATE 26-4-66
INITIALS C.A.C.

INSTRUCTION SHEET

SHEET No. 4 OF

L.S.A. No. AND NAME	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX. FAN OUT LOAD IN UNIT INPUTS			REMARKS.
			0 - 80°C	-20 - 80°C	-40 - 80°C	
12 CABLE RECEIVERS		2·0	31	30	26	USED FOLLOWING LSA 11 - FAN OUT CALC. WHEN CONNECTED TO LSA 11.
13 PULSE GENERATORS		2·4	17	16	14	1 INPUT = 3 UNIT INPUTS. Δ = 330 n.s. ± 10% USED WITH LSA 08.
14 PULSE GENERATOR		2·4	17	16	14	1 INPUT = 3 UNIT INPUTS. Δ = 680 n.s. ± 10% USED WITH LSA 08
15 2 I/P NAND GATE PLUS 2 INVERTING DRIVERS.		1·2	19	16	14	1 INPUT = 2·2 UNIT INPUTS. LARGER FAN OUT THAN LSA 01 ETC. 390 Ω PULL UP AT O/P PROVIDES GOOD +VE EDGES. SUITABLE FOR GATEING 100 ns. PULSE INTO REGISTERS.
		1·2	11	9	8	AS FOR LSA'S 01, 02 AND 03.
		1·2	19	16	14	1 INPUT = 2·2 UNIT INPUTS. LARGER FAN OUT THAN LSA 01 ETC. 390 Ω PULL UP AT O/P PROVIDES GOOD +VE EDGES. SUITABLE FOR GATEING 100 ns. PULSE INTO REGISTERS.
16 F-MINILOG DRIVERS.		1·2	9	8	7	1 INPUT = 1 UNIT INPUT.

GENERAL

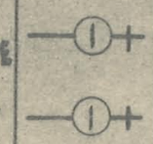
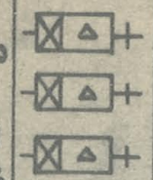
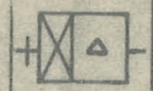
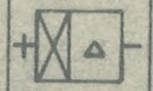
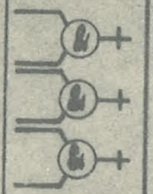


L.S.A. DESIGN NOTES.

ELLIOTT BROTHERS (LONDON) LTD.

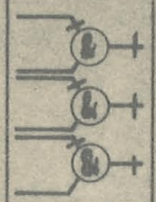
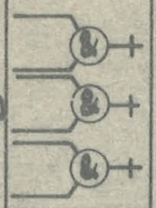
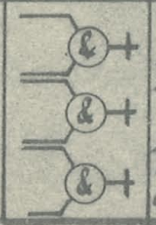
322A7191

DRAWN C.A.C. ISSUE No. 1
CHECKED CS456 A/C No. 1374
APPROVED DATE 26-4-66
DATE INITIAL C.A.C.

L.S.A. No. AND NAME	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX. FAN OUT LOAD IN UNIT INPUTS. 0-80°C	-20-80°C	-40-80°C	REMARKS.
						GENERAL +6V RAIL — 2·2K Ω ±5% A UNIT INPUT: — DIODE PURCH 101
17 PAPER TAPE RECEIVER.		2·0	30	29	25	USED FOLLOWING LSA 11 - FAN OUT CALC. WHEN CONNECTED TO LSA 11.
18 SINGLE I/P NOISE REJECTION INVERTORS		2·0	28	26	23	1 INPUT = 2·2 UNIT INPUTS. USUALLY USED FOLLOWING A KEY SWITCH TO AVOID SWITCH NOISE. Δ ≙ 1ms.
19 & 20 DELAY		3·0	20	19	17	1 INPUT = 1 UNIT INPUT. USUALLY USED IN POWER SUPPLY LOGIC. Δ ≙ 94ms.
19 & 21 DELAY		3·0	20	19	17	1 INPUT = 1 UNIT INPUT. USUALLY USED IN POWER SUPPLY LOGIC. Δ ≙ 22 m.s.
22 TWO I/P TRANSMI--TTERS.		0				1 INPUT = 2·2 UNIT INPUTS. USED PRECEEDING LSA 23. DATA O/P TO 50Ω COAX. MAY DRIVE UP TO 2 SELECTED AND 10 UNSELECTED LSA 23's.

INSTRUCTION SHEET

SHEET No. 5 OF

L.S.A. No. AND NAME	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX. FAN OUT LOAD IN UNIT INPUTS.			REMARKS.
			0-80°C	-20-80°C	-40-80°C	
23 GATED RECEIVERS		2·0	9	6	4	USED WITH L.S.A 22 28 & 44 DATA INPUT FROM 20' OF 30ns COAX GIVES DELAY FROM I/P LSA 22 TO O/P LSA 23 +VE EDGE IS TYPICALLY 80 n.s. (60n.s. DUE TO CABLE). -VE EDGE IS TYPICALLY 120 n.s. (60 n.s. DUE TO CABLE).
24-27	USED	BY D.P.D.				
28 2 I/P NAND GATES.		1·2	28	26	23	1 INPUT = 2·2 UNIT INPUTS. USED AS A SELECTION DRIVER FOR LSA 23. IN O/P LOADING CALC. A SELECTED LSA 23 = 4·0 UNIT INPUTS AND ANY O/P LOAD ON THE LSA 23 SHOULD BE ADDED TO LSA 28 TOTAL.
43 VOLTAGE RAIL SENSING			1	1	1	
44 2 I/P NAND GATES		1, 3, 5 } 1·9 2, 4, 6 } 1·2	11	9	8	AS FOR LSA 01, 02 & 03 INPUTS 1, 3 & 5 HAVE A HIGH THRESHOLD FOR USE FOLLOWING AN L.S.A 23

GENERAL. +6V RAIL — 2·2KΩ ± 5% — A UNIT INPUT = DIODE PURCH 101

L.S.A. DESIGN NOTES.

322A 7191

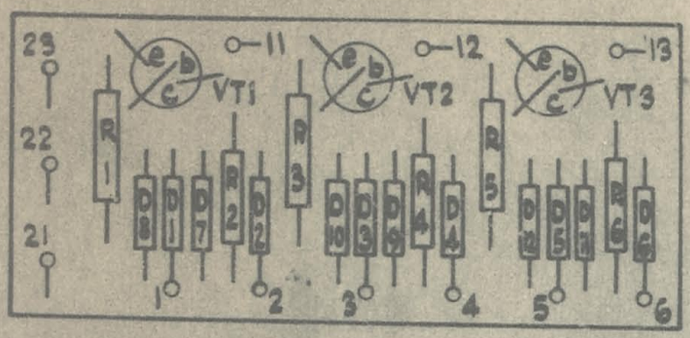
SHEET No. 6 OF

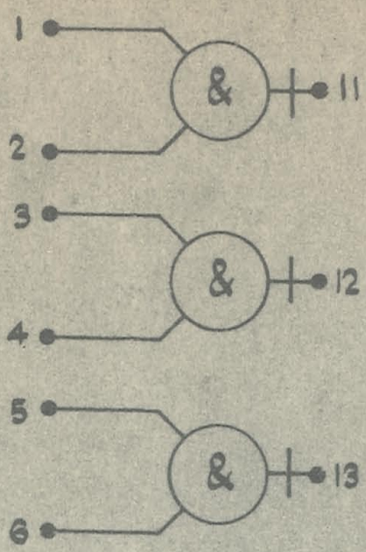
TITLE

ELLIOTT BROTHERS (LONDON) LTD.

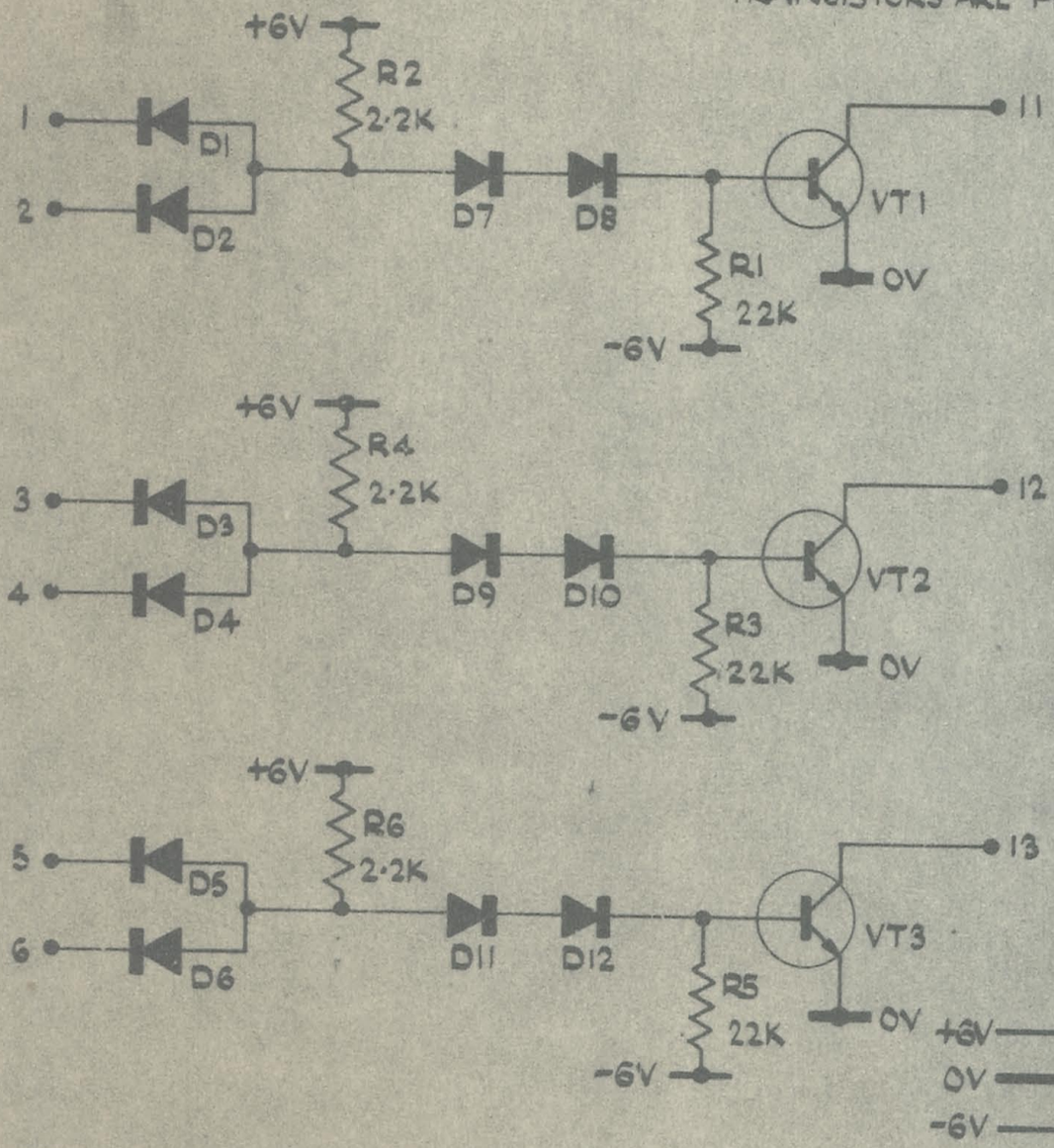
INSTRUCTION SHEET

DRAWN	C.A.C.	ISSUE No.	1 2 3
CHECKED	CS/456	A.R. No.	1374 1588 1796
APPROVED		DATE	26-4-66 26-8-66 26.11.66
DATE	16/5/66	INITIALS	C.A.C. KG





DIODES ARE PURCH. 101
TRANSISTORS ARE PURCH. 100



DRAWN C.A.C.	ISSUE No. 1		
CHECKED CS 456	A.R. No. 1374		
APPROVED	DATE 26-4-66		
DATE 16.5.66	INITIAL C.A.C.		

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

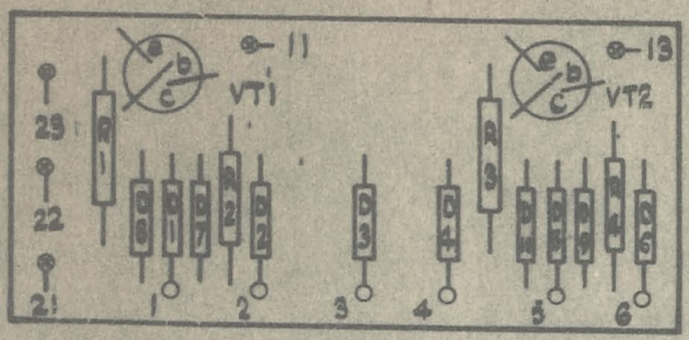
LSA 01

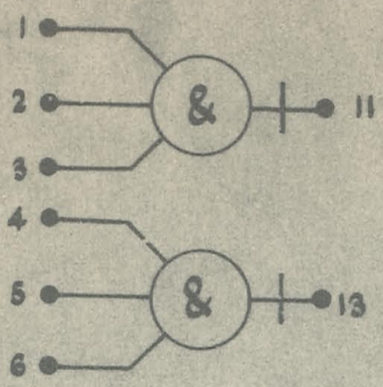
2-INPUT NAND GATE 920B

INSTRUCTION SHEET

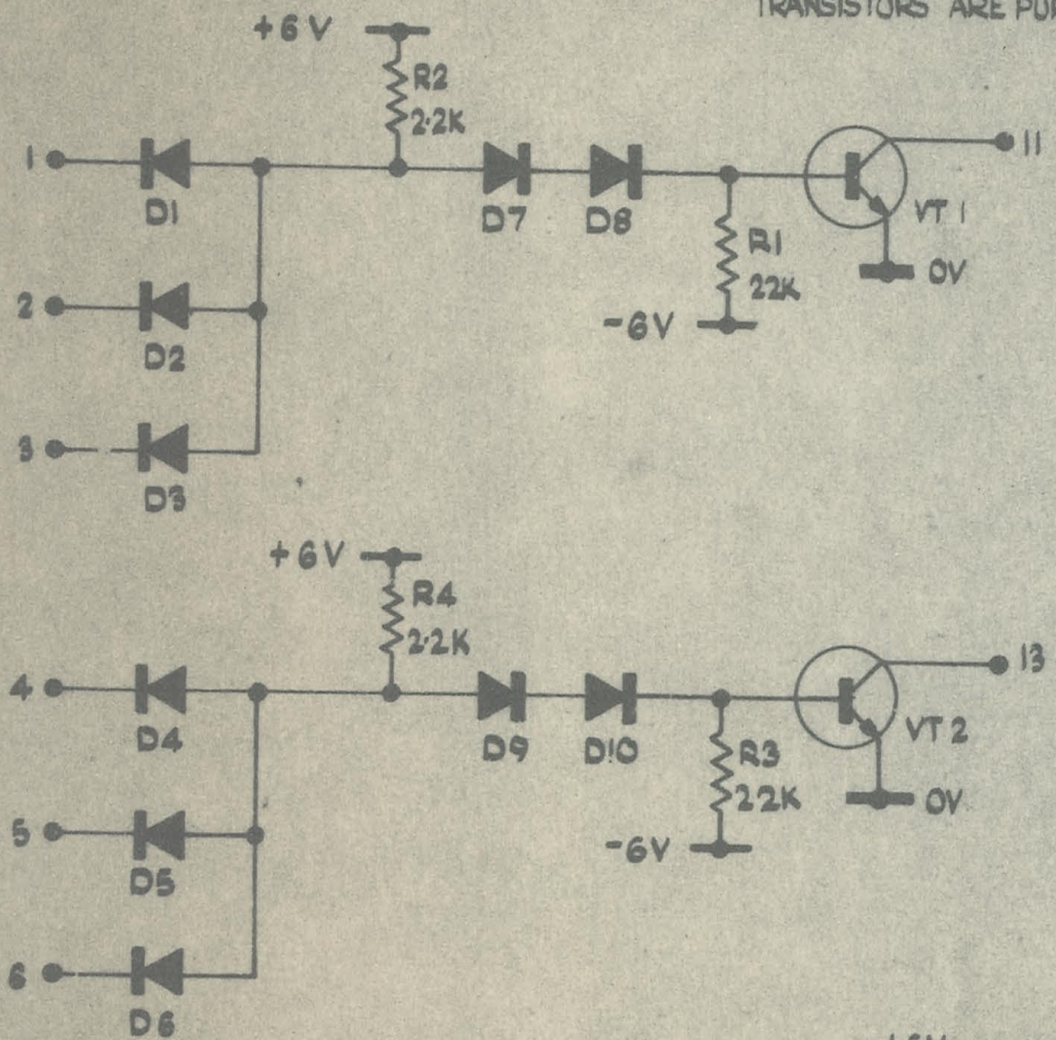
322A7191

SHEET No. 7 OF





DIODES ARE PURCH.101
TRANSISTORS ARE PURCH 100.



+6V — 21
0V — 23
-6V — 22

DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No	1374
APPR'VED	ERM	DATE	26-4-66
DATE	6/5/66	INITIALS	C.A.C.

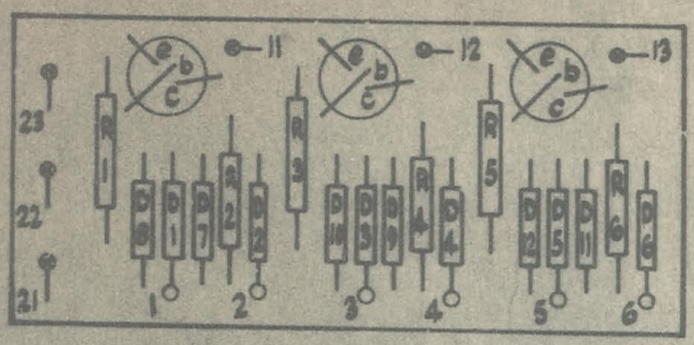
ELLIOTT BROTHERS (LONDON) LTD.

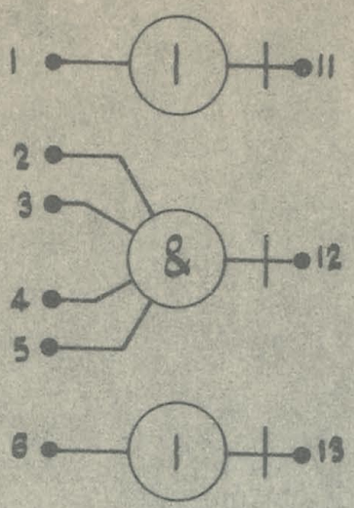
TITLE

L.S.A. 02.
3 - INPUT NAND GATE 920 B

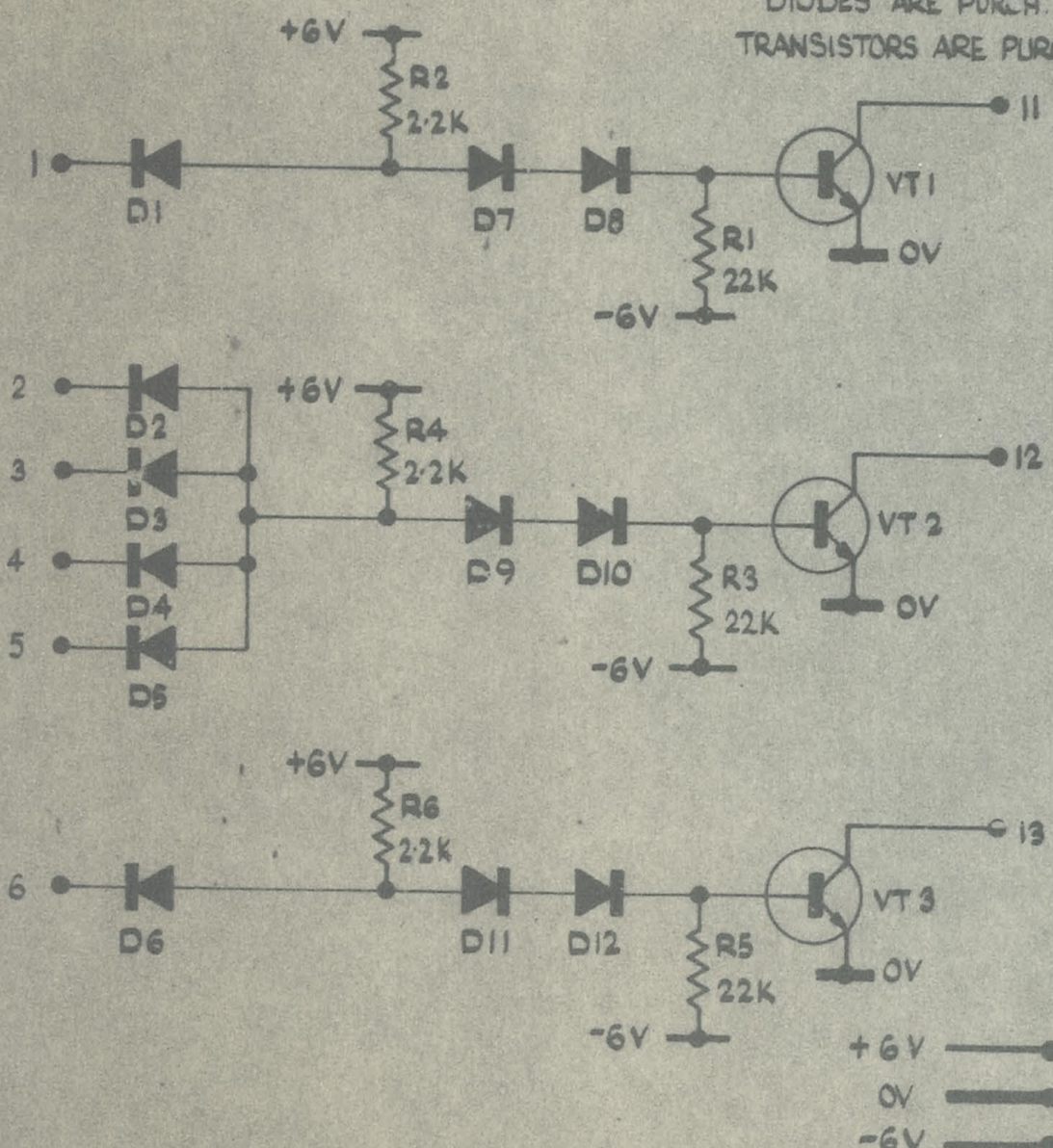
INSTRUCTION SHEET
322A7191

SHEET No 8
OF





DIODES ARE PURCH. 101
TRANSISTORS ARE PURCH 100



DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No	1374
APPROVED		DATE	26-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

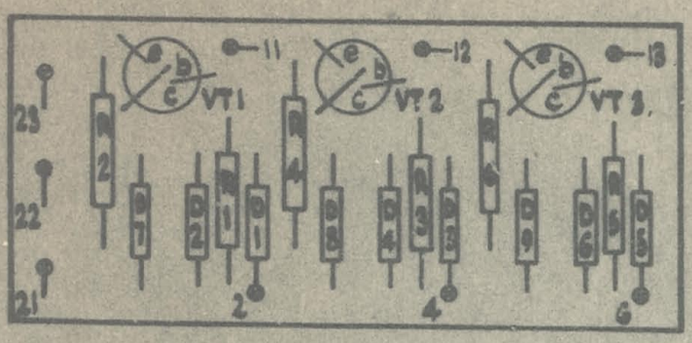
L.S.A. 03

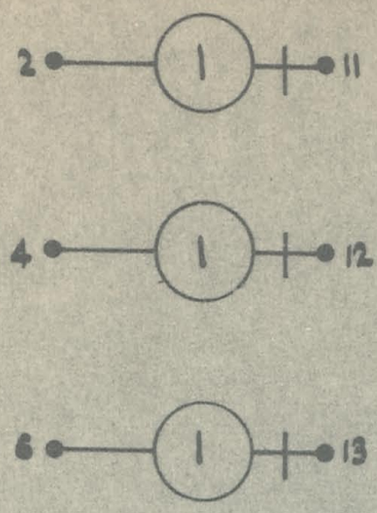
4-INPUT NAND GATE + 2 INVERTERS 9208

INSTRUCTION SHEET

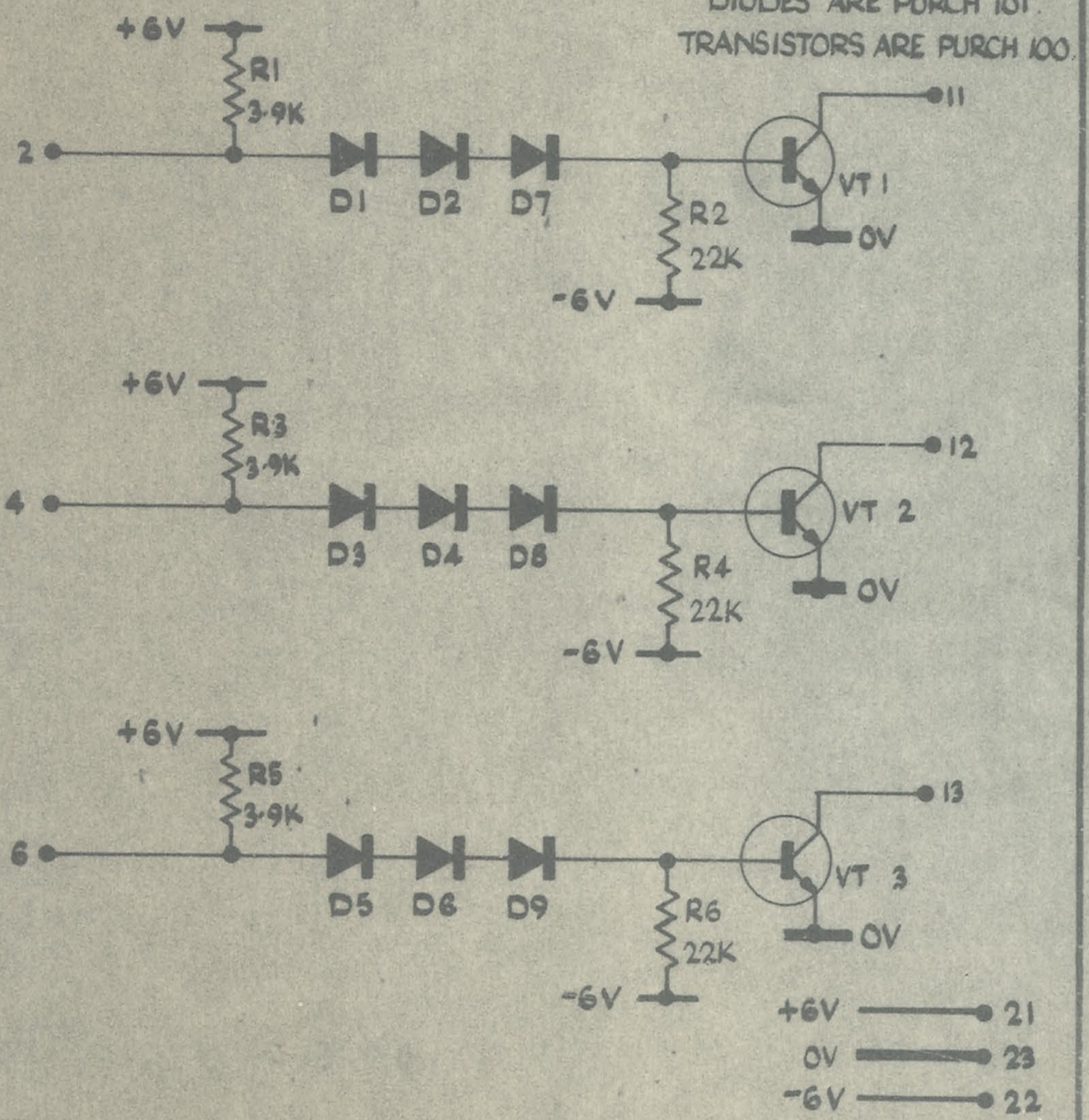
322A7191

SHEET No 9 OF





DIODES ARE PURCH 101.
TRANSISTORS ARE PURCH 100.



DRAWN C.A.C.	ISSUE No. 1	
CHECKED CS 456	A.R. No 1374	
APPR'VED	DATE 26-4-66	
DATE	INITIALS C.A.C.	

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

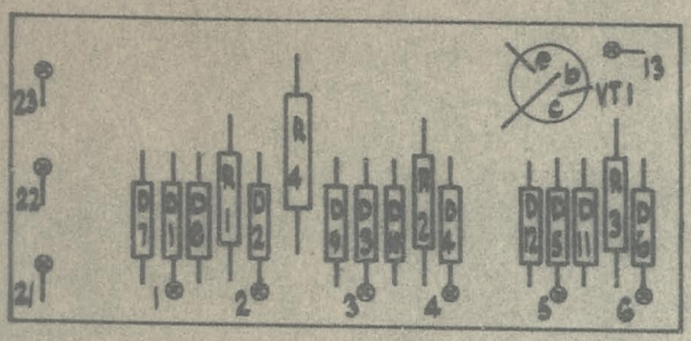
L.S.A. 04

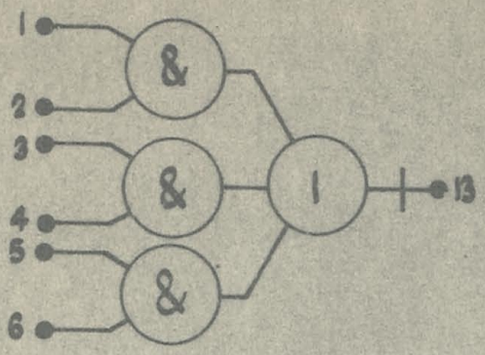
CONTROL MATRIX WAVFORM AMPLIFIERS 9208

INSTRUCTION SHEET

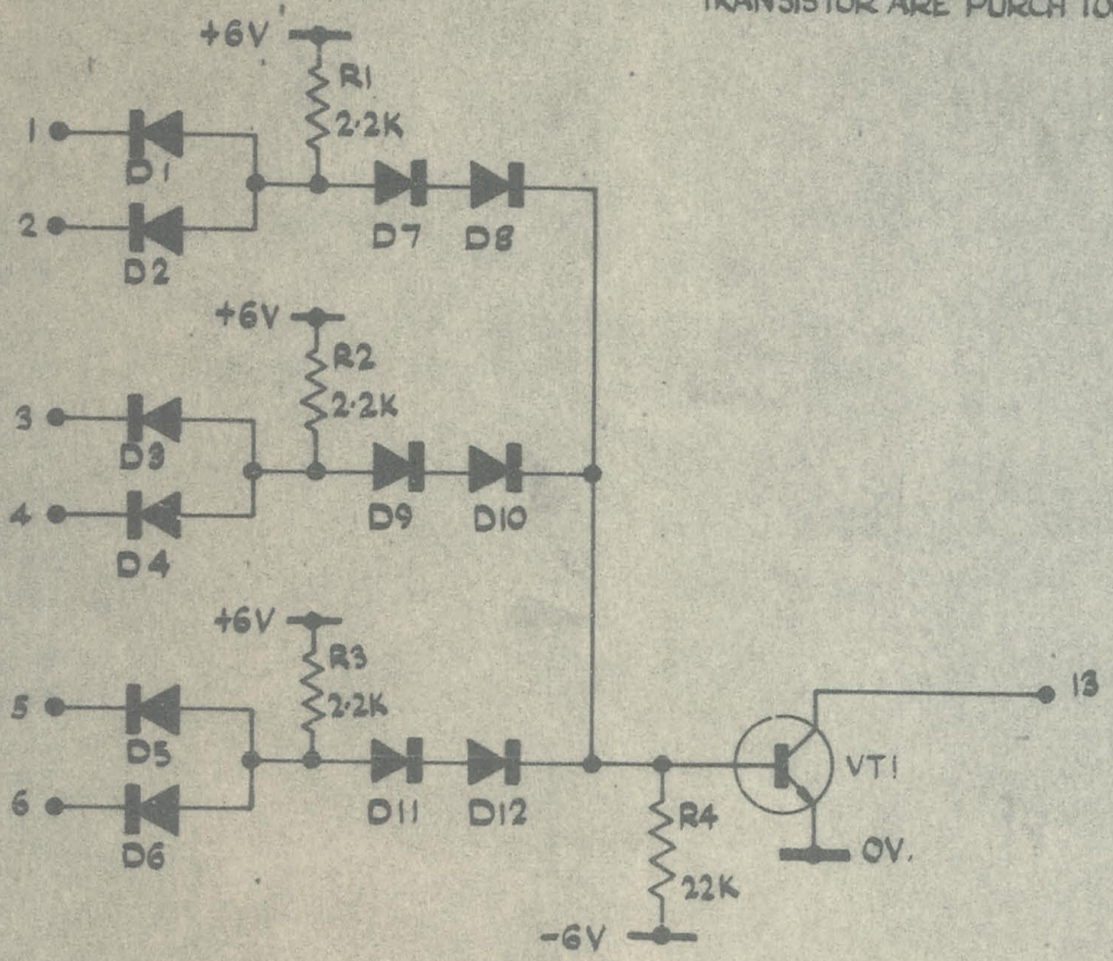
322 A7191

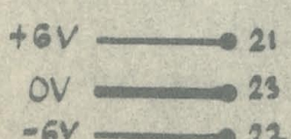
SHEET No 10 OF





DIODES ARE PURCH 101
TRANSISTOR ARE PURCH 100.



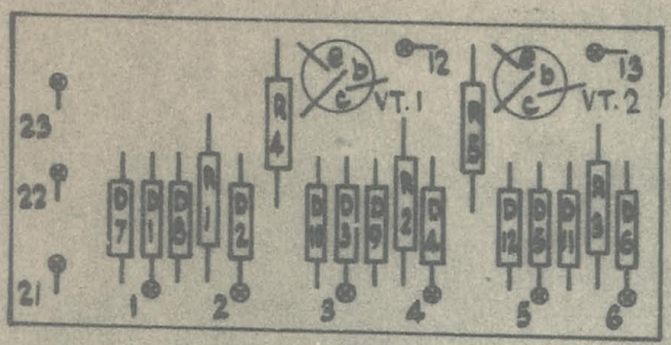


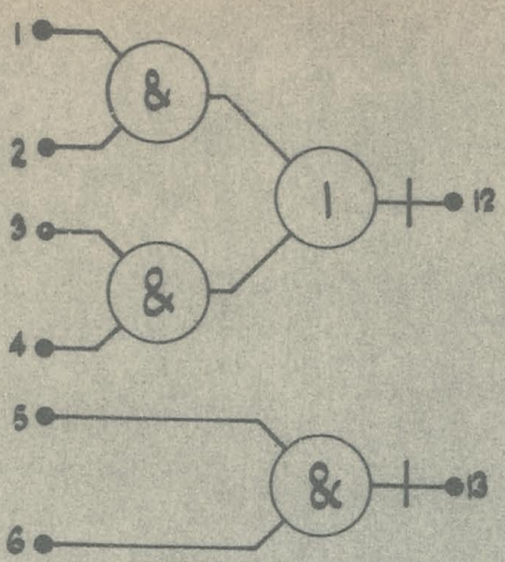
DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No	1374
APPR VED	Elliott	DATE	26-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

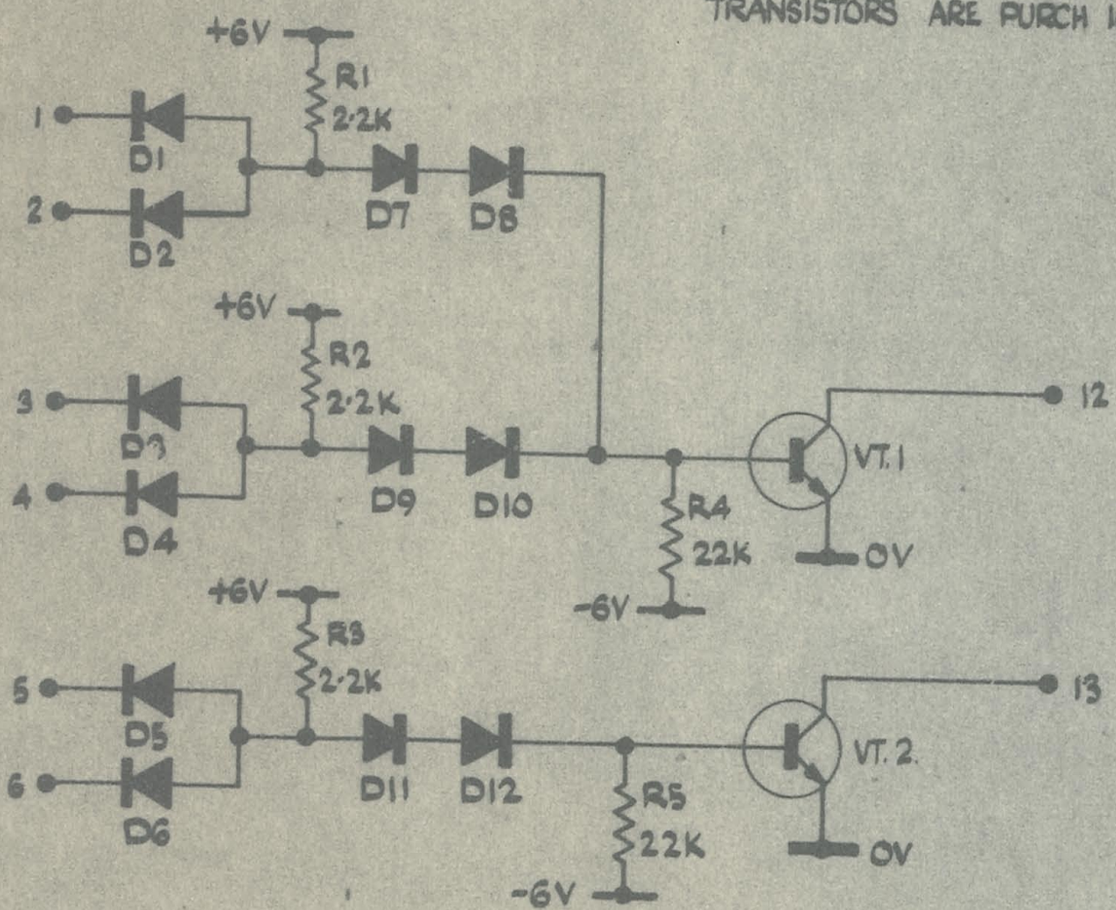
TITLE	L.S.A. 05 9208.	INSTRUCTION SHEET 322A 7191

SHEET No 11
OF





DIODES ARE PURCH 101.
TRANSISTORS ARE PURCH 100.



+6V — 21
0V — 23
-6V — 22

DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No	1374
APPR VED		DATE	25-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

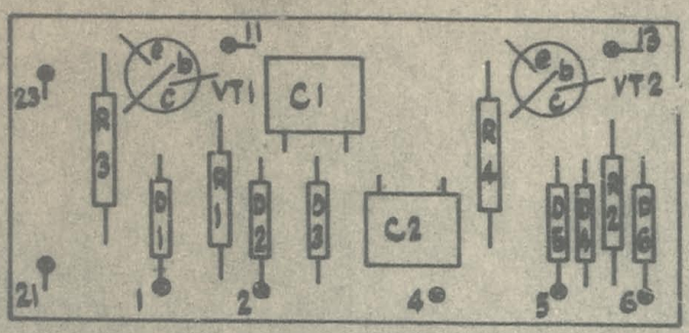
TITLE

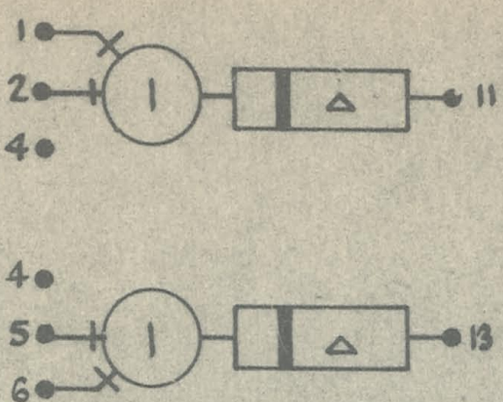
L.S.A. 06
9208

INSTRUCTION SHEET

322A7191

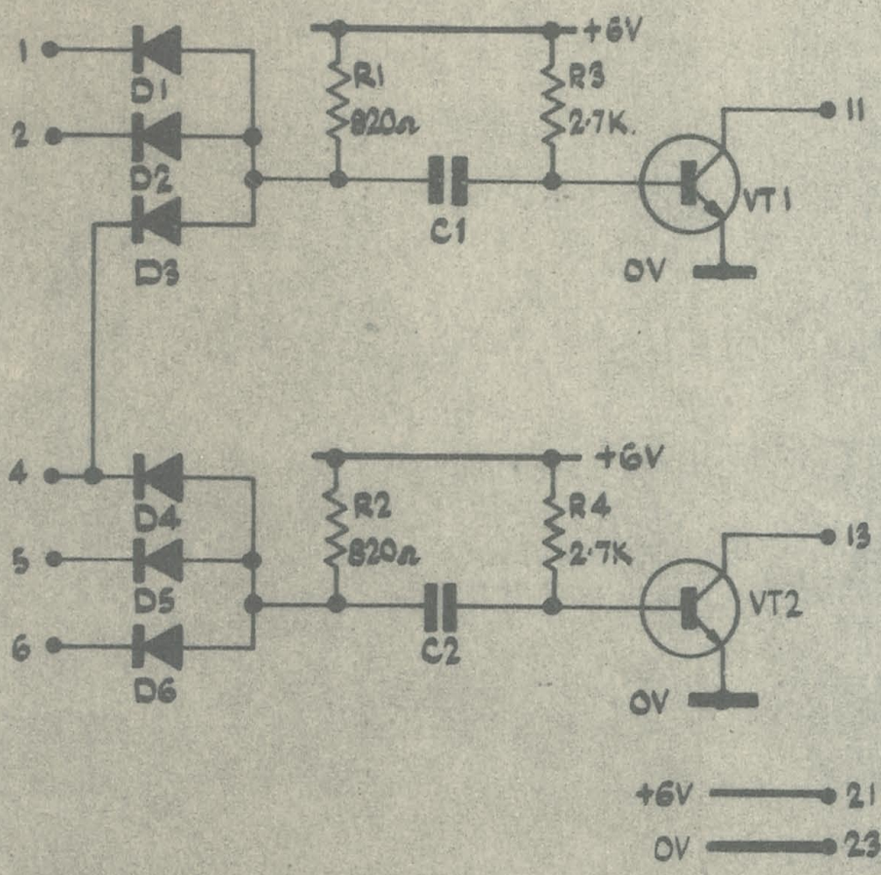
SHEET No. 12
OF





PULSE WIDTH (Δ) = CRS (WHERE C = CAPACITANCE IN pF.)

DIODES ARE PURCH 101.
TRANSISTORS ARE PURCH 100



LSA. No.	C_1	C_2
07	100	100
13	330	330
34	100	330

NOTE:-

PULSE WIDTH (+VE). PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR GREATER THAN N/2 SEC. I/P 4 — 2·4 V. REFERENCE VOLTAGE.

DRAWN	C.A.C.	ISSUE No.	1 2
CHECKED	CS 456	A.R. No	1374 1505
APPROVED		DATE	26-4-6629-666
DATE	16/5/66	INITIALS	C.A.C. R.W.C.

ELLIOTT BROTHERS (LONDON) LTD.

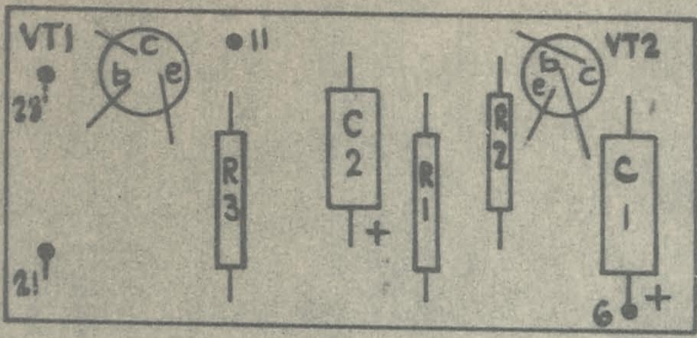
TITLE

L.S.A. 07, 13, 34
PULSE GENERATORS. 920B

INSTRUCTION SHEET

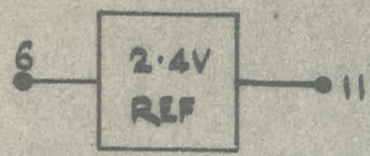
322A 7191

SHEET No 13
OF

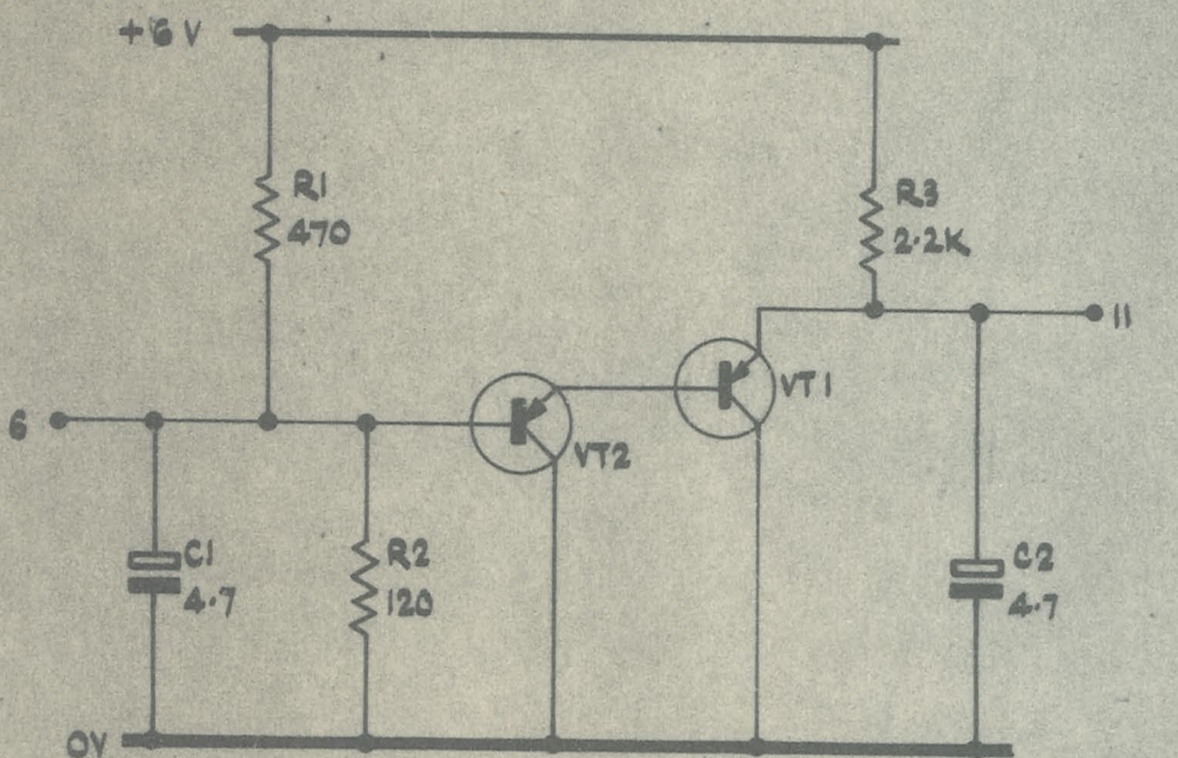


I/P 6 VARIES O/P 11 VOLTAGE FOR MARGINAL TEST.

O/P 11 PROVIDES 2·4V REF.



TRANSISTORS ARE MM 2712



+6V — 21

OV — 23

DRAWN	C.A.C.	ISSUE No.	1	2
CHECKED	CS 456	A.R. No	1374	1505
APPR'VED	[illegible]	DATE	26·4·66	29·6·66
DATE	16/5/66	INITIALS	C.A.C.	R.W.C

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

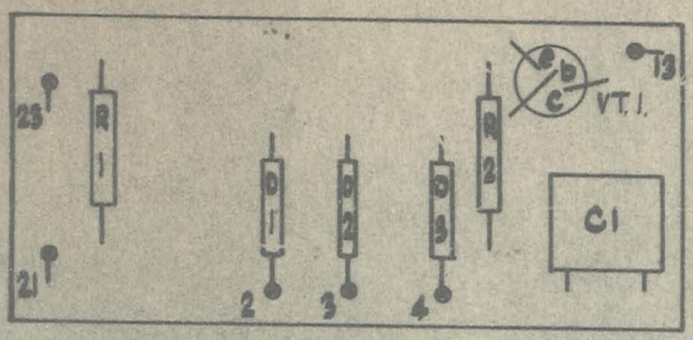
L.S.A. 08

VOLTAGE REFERENCE 9208

INSTRUCTION SHEET

322A7191

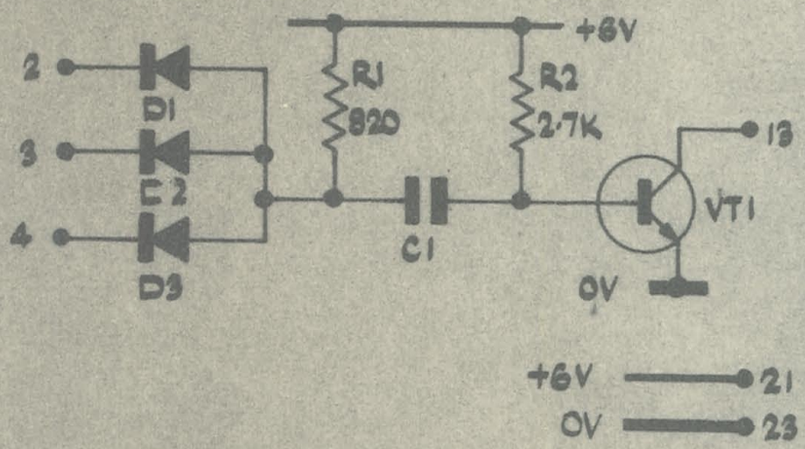
SHEET No 14 OF



PULSE WIDTH (Δ) = Cms. (WHERE C = CAPACITANCE IN pF)

DIODES ARE PURCH 101.
TRANSISTORS ARE PURCH 100.

LSA. No.	C1	
09	470	
14	680	



NOTE:-

PULSE WIDTH (+VE). PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR > N/2 SEC.

I/P 4 — 2·4V REFERENCE VOLTAGE.

DRAWN	C.A.C.	ISSUE No.	1 2
CHECKED	CS 456	A.R. No	1374 1505
APPROVED	[illegible]	DATE	26-4-66 29-6-66
DATE	16/5/66	INITIALS	C.A.C. R.W.C

ELLIOTT BROTHERS (LONDON) LTD.

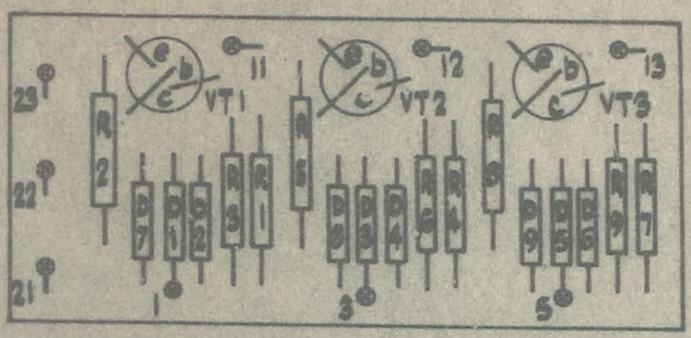
TITLE

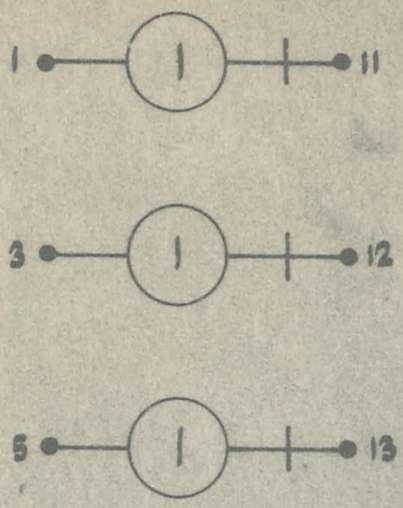
L.S.A. 09, 14,
PULSE GENERATOR, 920B

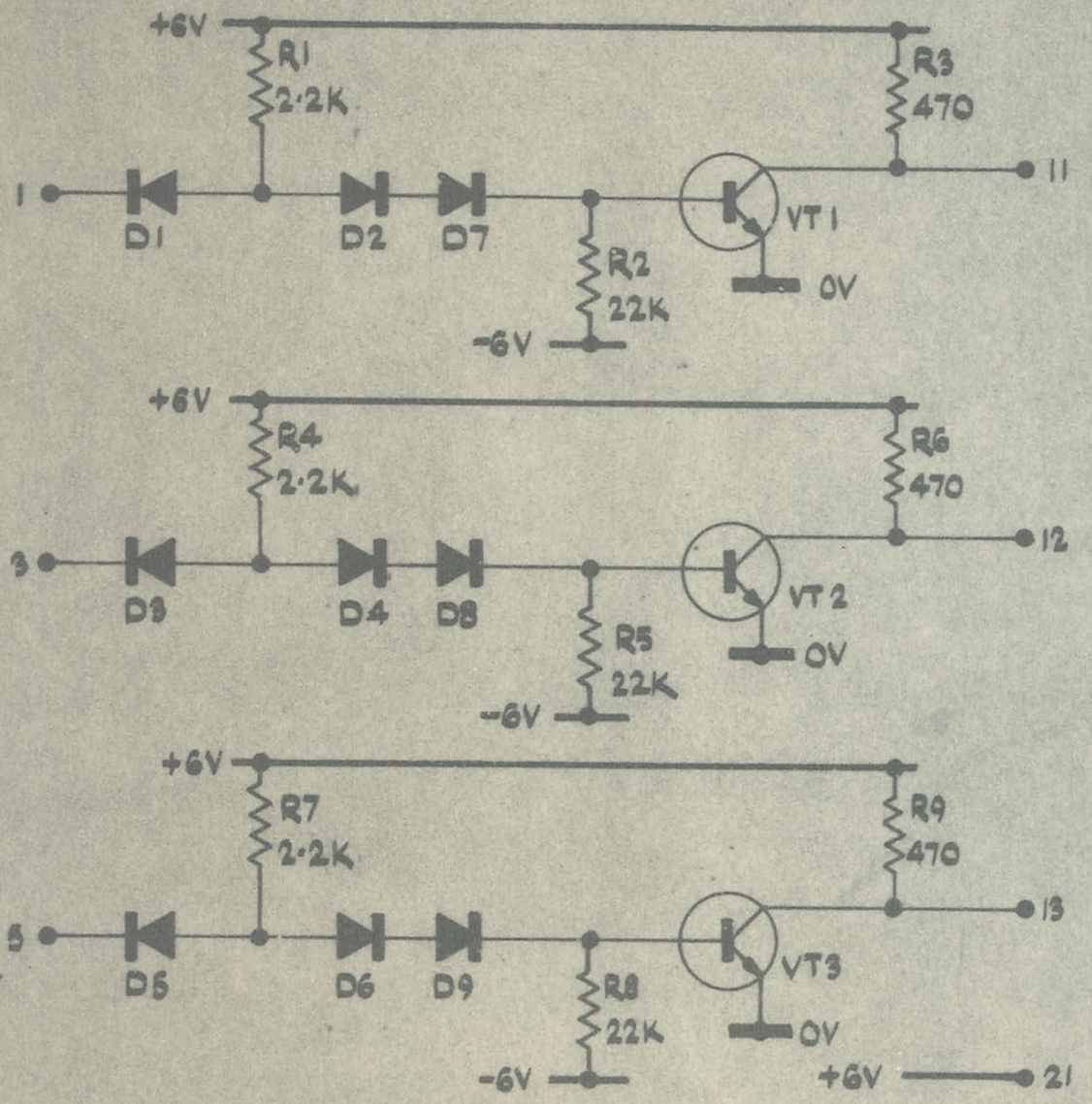
INSTRUCTION SHEET

322A 7191

SHEET No 15
OF







DIODES ARE PURCH 101.
TRANSISTORS ARE PURCH 100.

DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No.	1374
APPR'VED	[illegible]	DATE	26-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

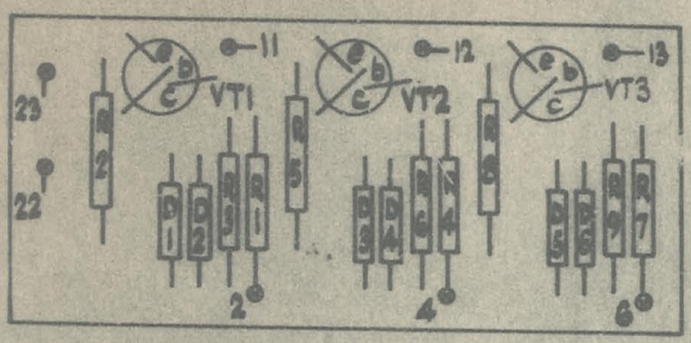
TITLE

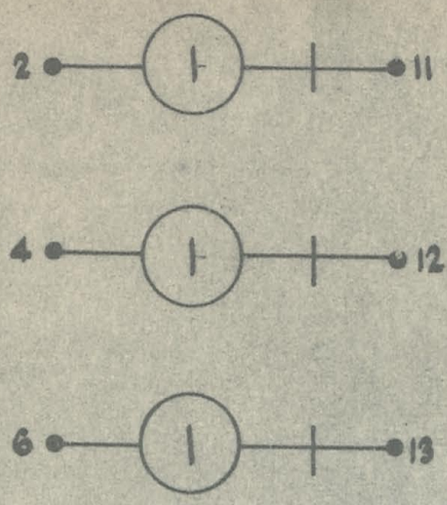
L.S.A. 11
CABLE TRANSMITTERS '9208

INSTRUCTION SHEET

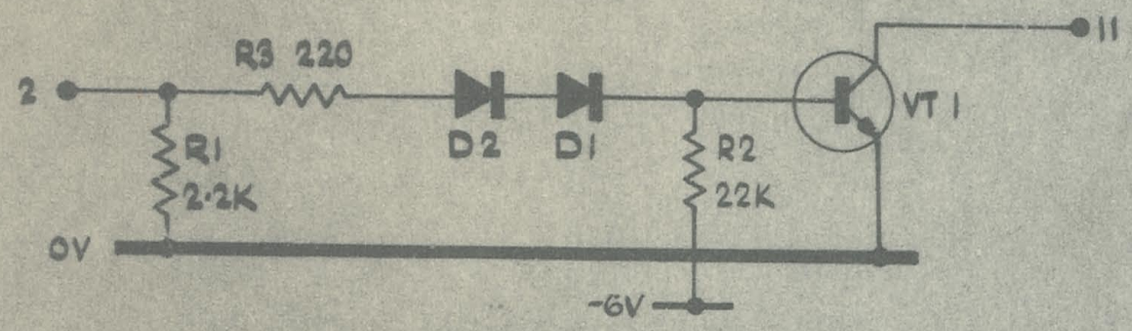
322A7191

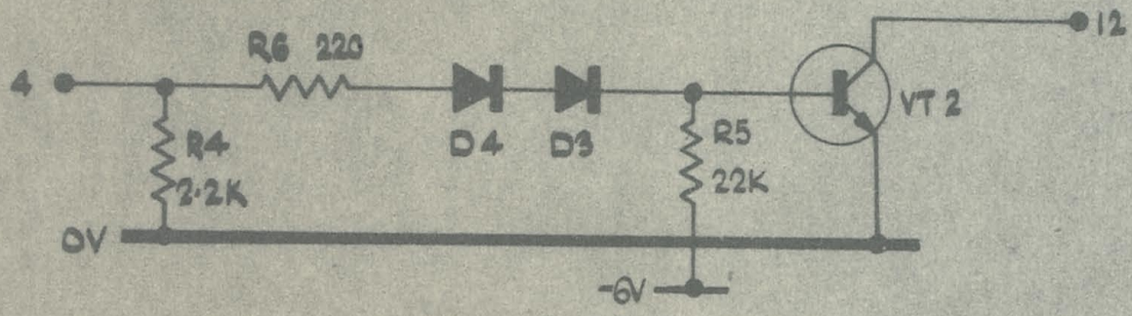
SHEET No 16
OF

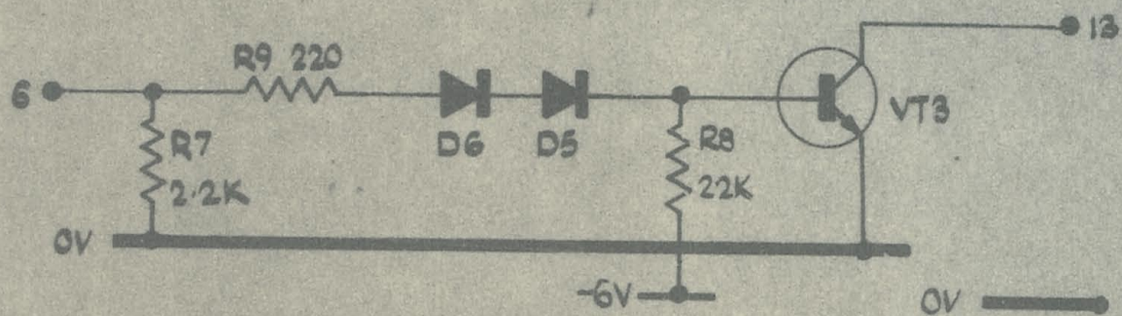


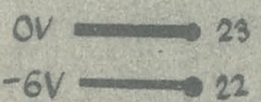


DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100









DRAWN C.A.C.	ISSUE No. 1
CHECKED CB 456	A.R. No 1374
APPR'VED E.R.W.	DATE 26-4-66
DATE 16/5/66	INITIALS C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

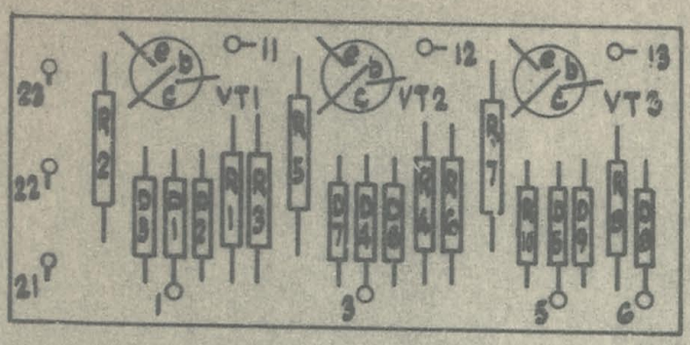
TITLE

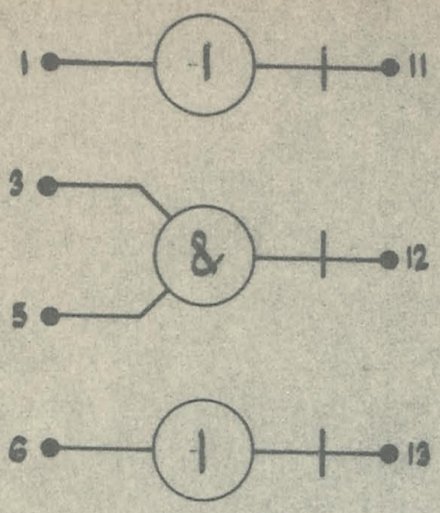
L.S.A. 12.
CABLE RECEIVERS 920B

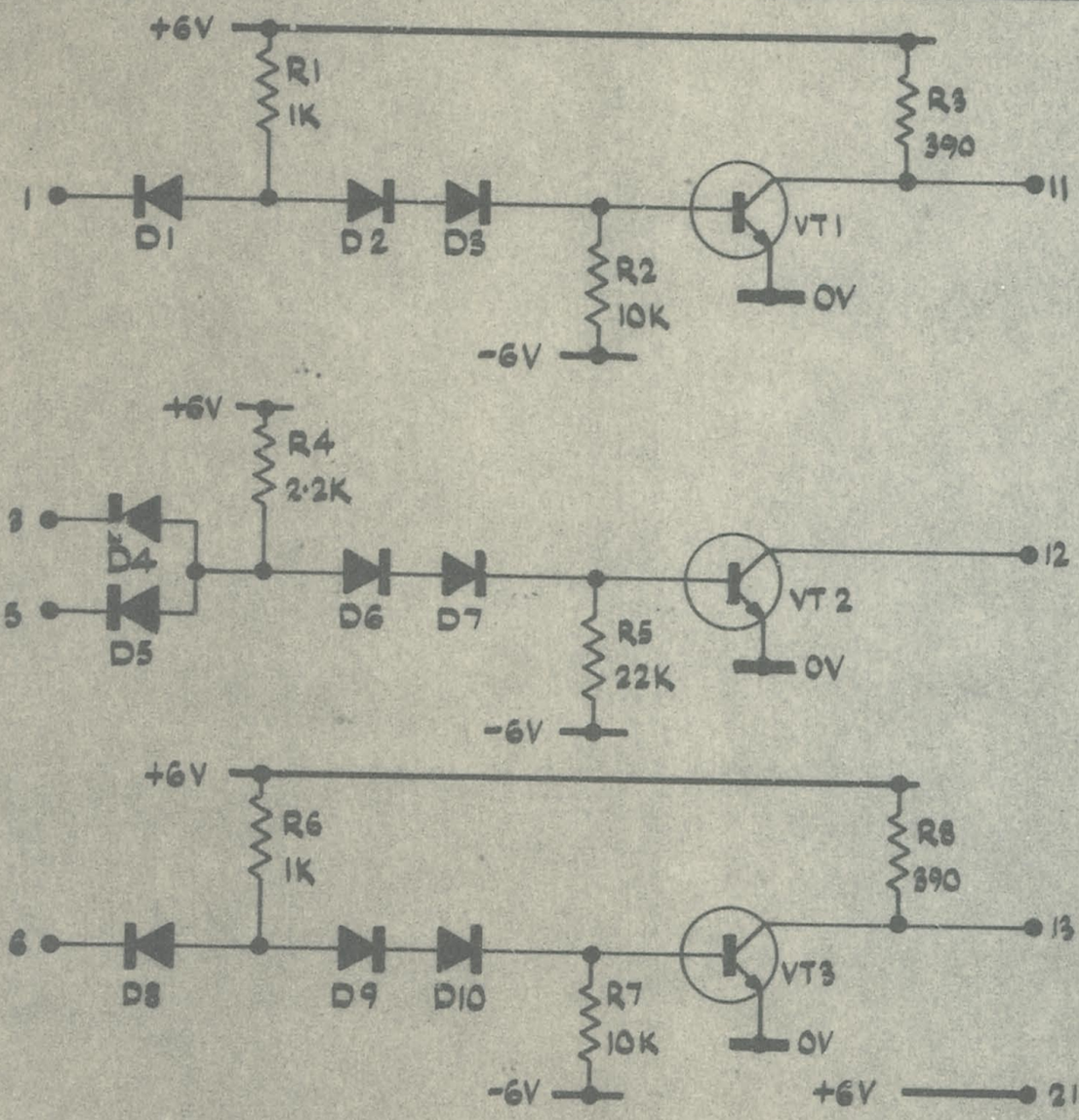
INSTRUCTION SHEET

322A7191

SHEET No 17
OF







DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100

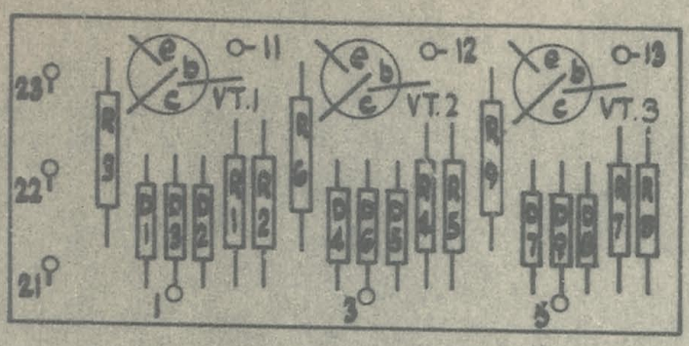
DRAWN C.A.C.	ISSUE No. 1												
CHECKED CS 456	A.R. No 1374												
APPR VED	DATE 26-4-66												
DATE 16/5/66	INITIALS C.A.C.												

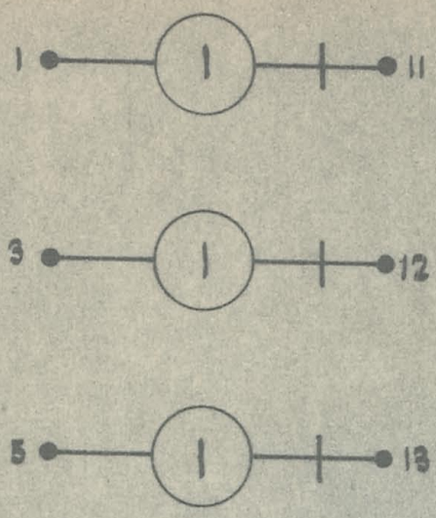
ELLIOTT BROTHERS (LONDON) LTD.

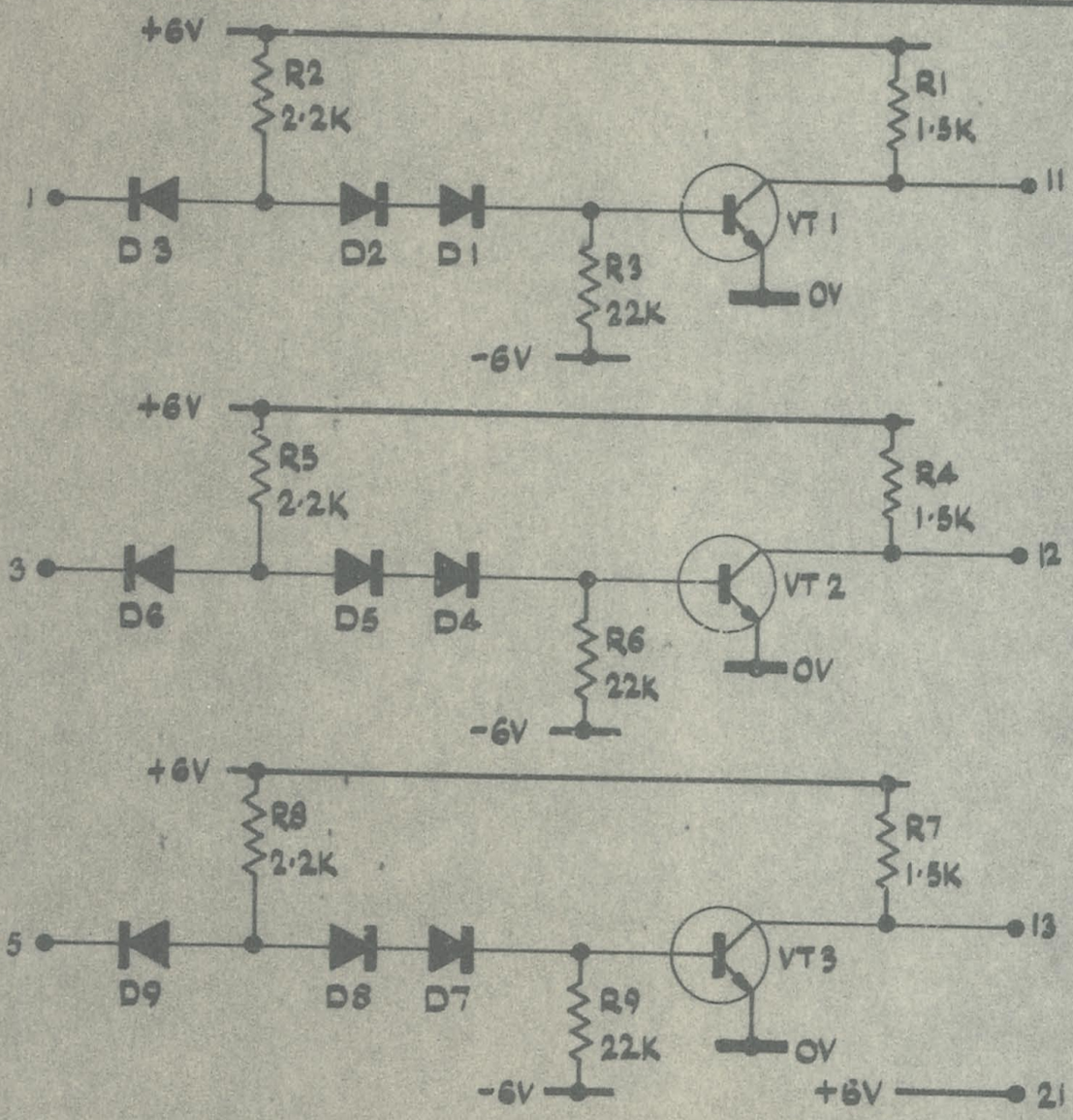
TITLE
L.S.A. 15 920B
2-INPUT NAND GATE + 2 INVERTING DRIVERS

INSTRUCTION SHEET
322A7191

SHEET No 18 OF







DIODES ARE PURCH 101

TRANSISTORS ARE PURCH 100.

DRAWN C.A.C.	ISSUE No. 1		
CHECKED CS 4-66	A.R. No 1374		
APPROVED [illegible]	DATE 26-4-66		
DATE 16/5/66	INITIALS C.A.C.		

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

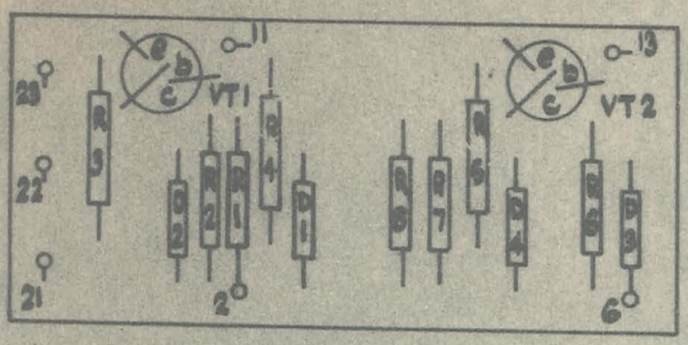
L.S.A. 16.

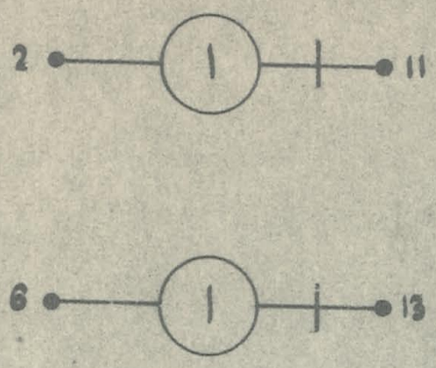
F- MINILOG DRIVERS 9206

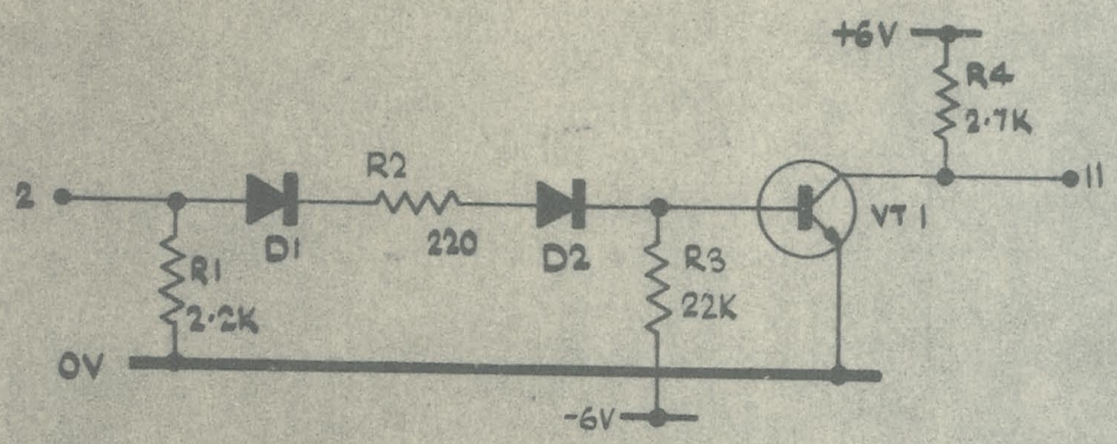
INSTRUCTION SHEET

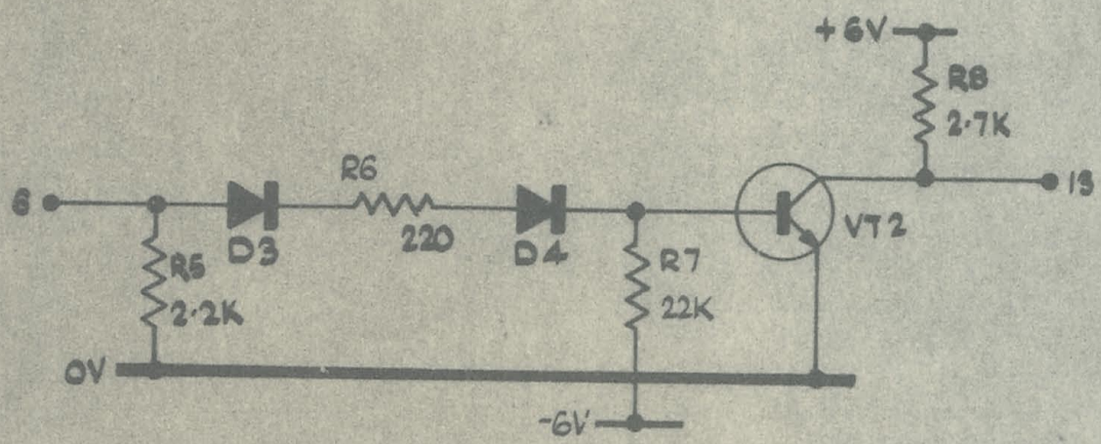
322A7191

SHEET No 19 OF









DIODES ARE PURCH 101

TRANSISTORS ARE PURCH 100.

+6V — 21

0V — 23

-6V — 22

DRAWN C.A.C.	ISSUE No. 1	2
CHECKED CS 456	A.R. No 1374	1505
APPROVED	DATE 26-4-66	29-6-66
DATE 16/1/67	INITIALS C.A.C.	R.W.C

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

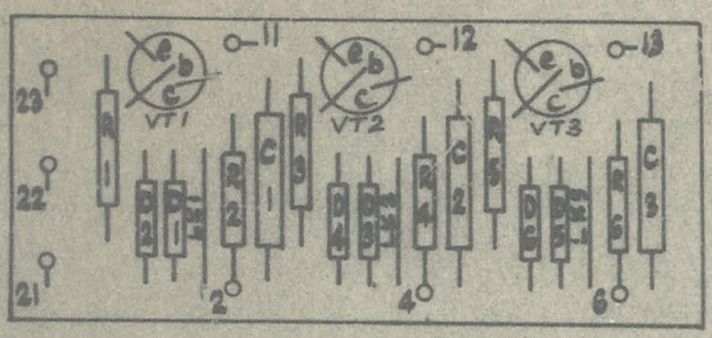
L.S.A. 17.

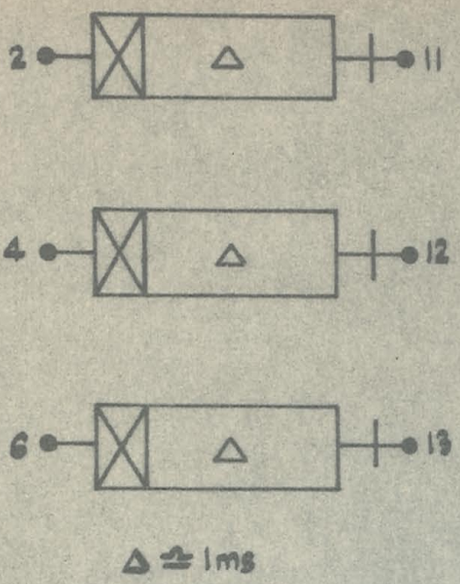
PAPER TAPE RECEIVER 9208.

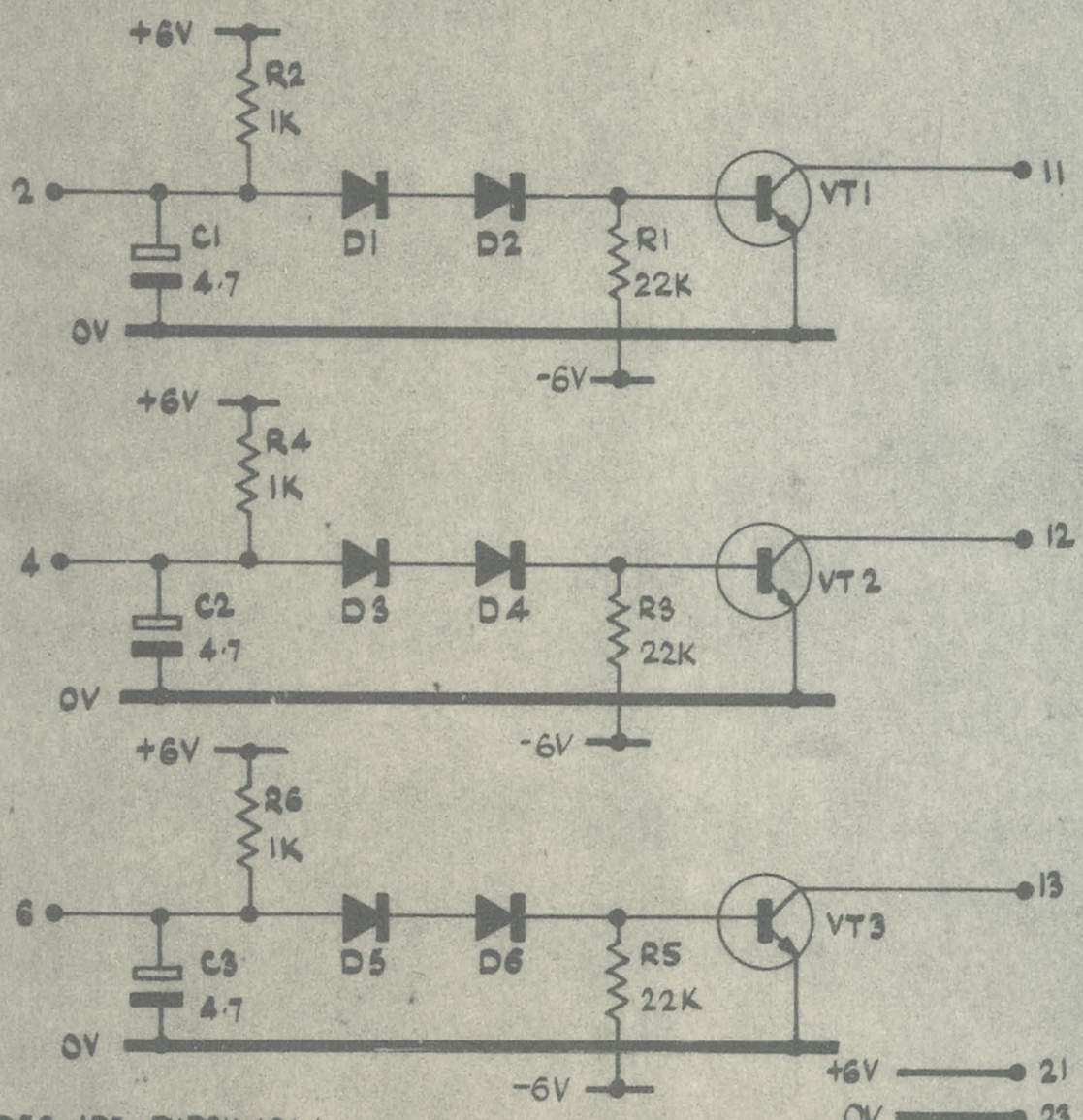
INSTRUCTION SHEET

322A 7191

SHEET No 20 OF







DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100

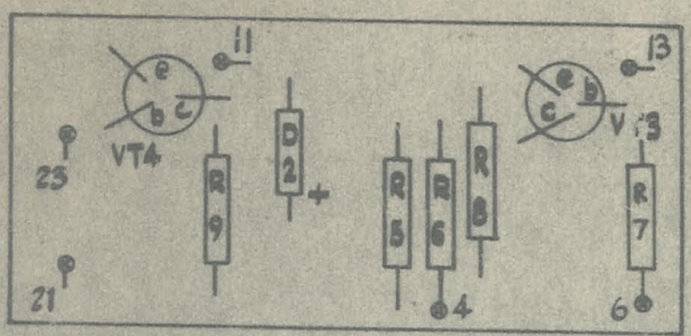
DRAWN	C.A.C.	ISSUE No.	1 2
CHECKED	CS 456	A.R. No	1374 1505
APPROVED	E.R.K.	DATE	26·4·66 29·6·66
DATE	16/5/66	INITIALS	C.A.C. R.W.C

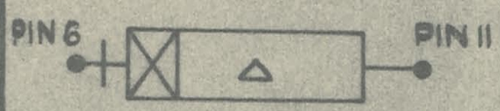
ELLIOTT BROTHERS (LONDON) LTD.

TITLE
L.S.A. 18.
SINGLE I/P NOISE REJECTION INVERTER. 9208

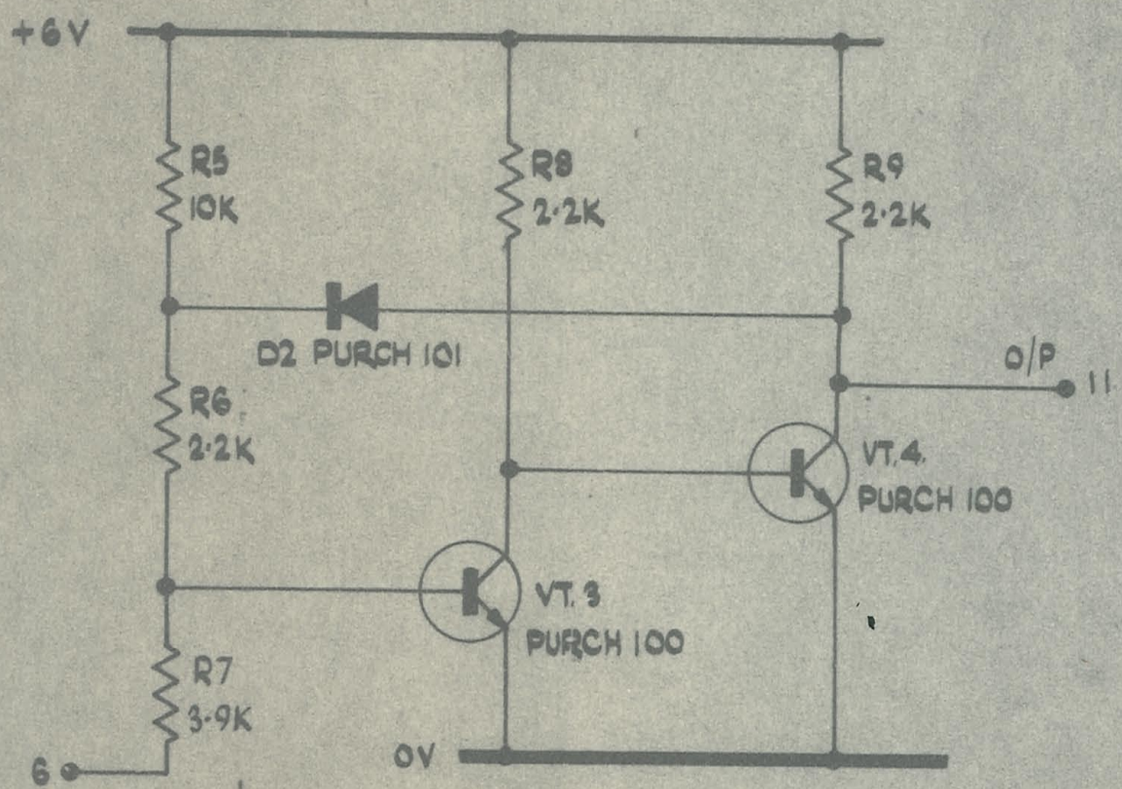
INSTRUCTION SHEET
322A7191

SHEET No 21
OF





ONLY USED FOLLOWING LSA. 20 OR 21. COMBINATION CIRCUIT GIVES DELAY (Δ) ≈ 10ms/μF WHERE μF IS CAPACITANCE OF LSA 20 OR LSA 21.



DIODE IS PURCH 101
TRANSISTORS ARE PURCH 100

+6V —— 21
0V —— 23

DRAWN	C.A.C.	ISSUE No.	1 2
CHECKED	CS 456	A.R. No	1374 1505
APPR VED	RWC	DATE	26-4-66 8·7·66
DATE	16/5/66	INITIALS	C.A.C. R.W.C.

ELLIOTT BROTHERS (LONDON) LTD.

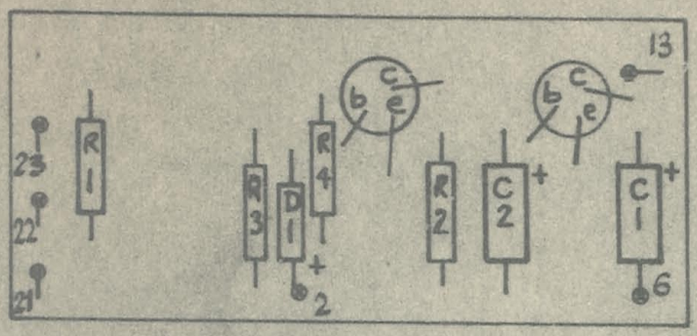
TITLE

L.S.A. 19
DELAY 920B

INSTRUCTION SHEET

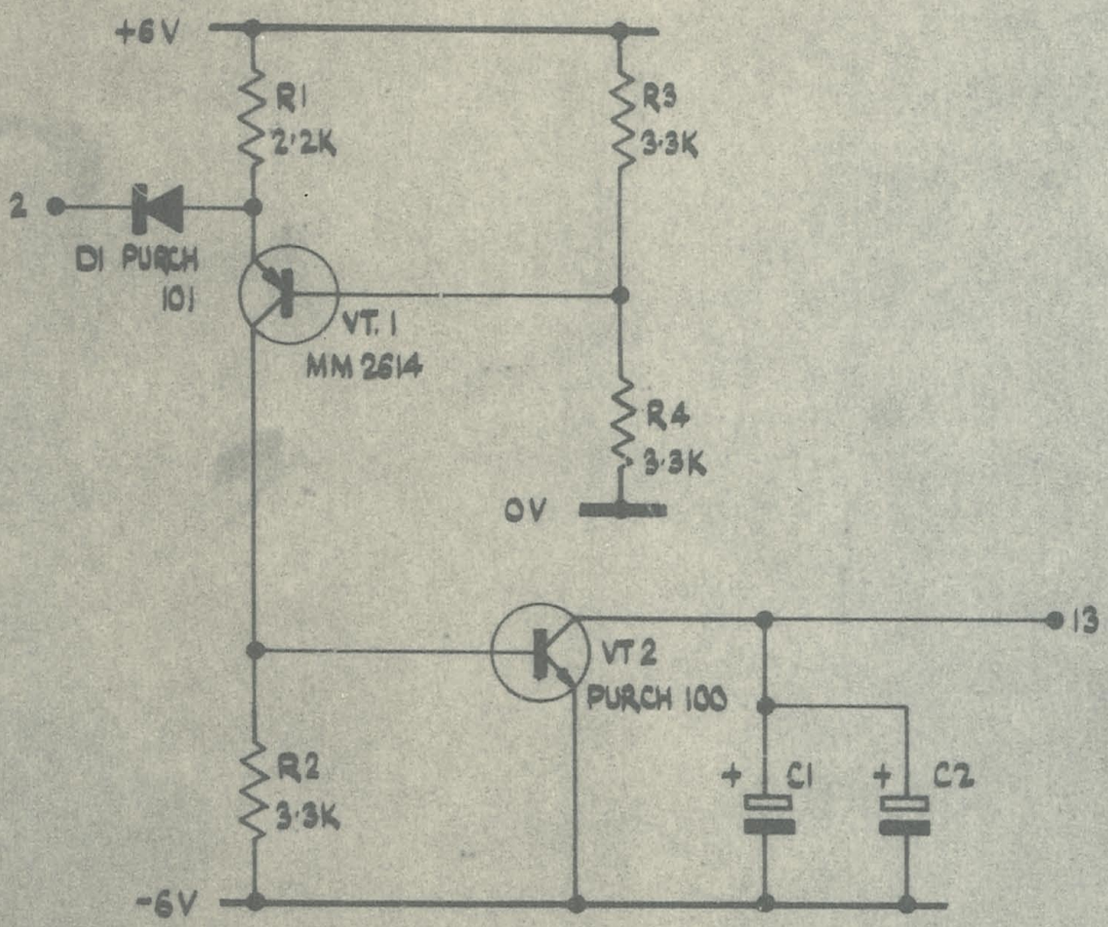
322A7191

SHEET No 22 OF



ONLY USED PRECEEDING L.S.A. 19. OVERALL DELAY ≏ 10 ms/μF WHERE μF IS CAPACITANCE OF $C_1 + C_2$

2 ——— 13



ELEMENT	C1	C2
LSA 20	4·7 μF	4·7 μF
LSA 24	2·2 μF	1·0 μF
LSA 25	2·2 μF	·047 μF

+6V ——— 21
0V ——— 23
-6V ——— 22

DRAWN C.A.C.	ISSUE No.	1	2								
CHECKED CS 456	A.R. No	1374	1505								
APPROVED [illegible]	DATE	26-4-66	29-6-66								
DATE 16/5/66	INITIALS	C.A.C.	R.W.C								

ELLIOTT BROTHERS (LONDON) LTD.

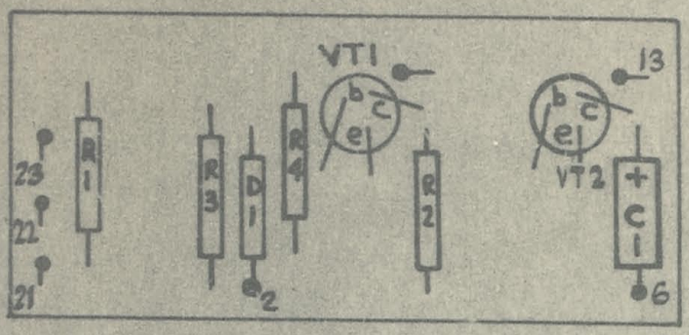
TITLE

L.S.A. 20, 24, 25. DELAY.

INSTRUCTION SHEET

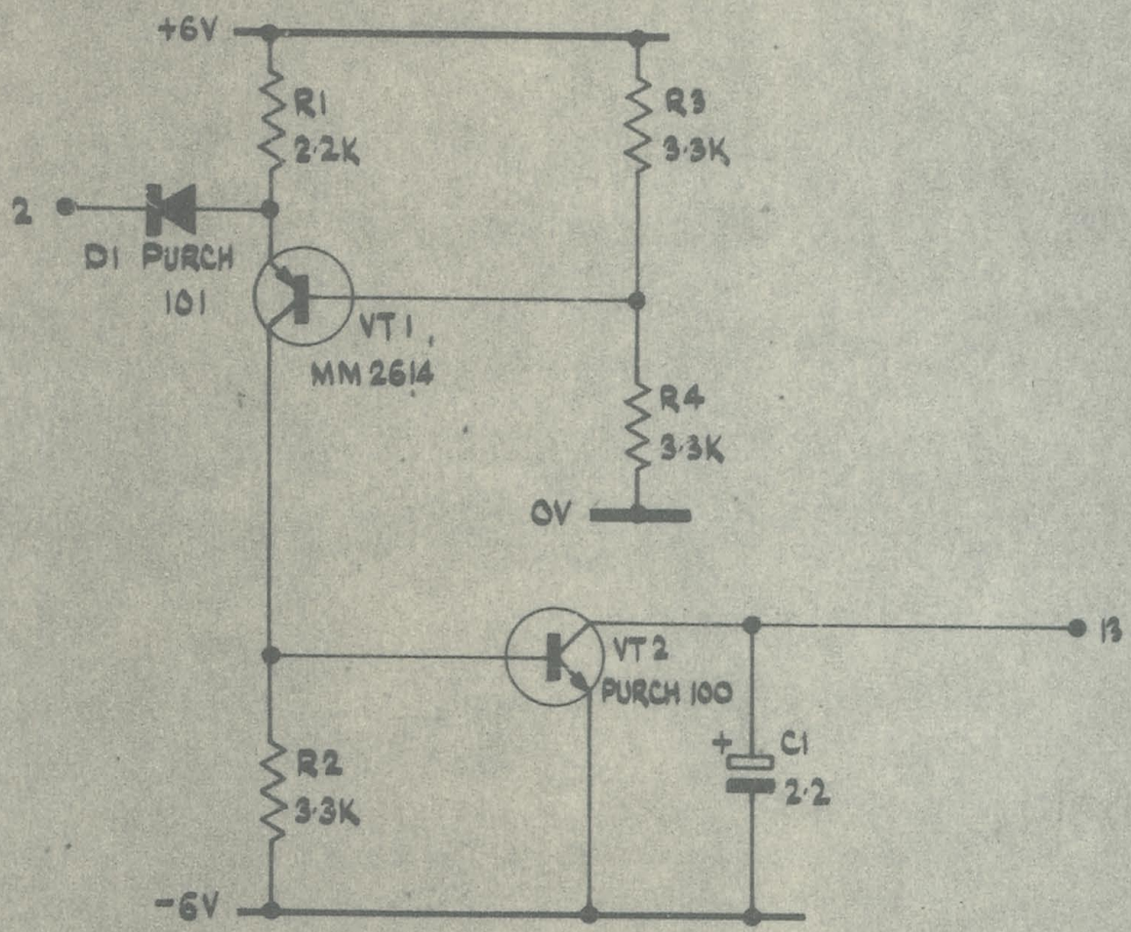
322A7191

SHEET No. 23 OF



ONLY USED PRECEEDING L.S.A 19. OVERALL DELAY ≙ 10 m.s/μF WHERE μF IS CAPACITANCE OF C_1.

2 ● ——— ● 13

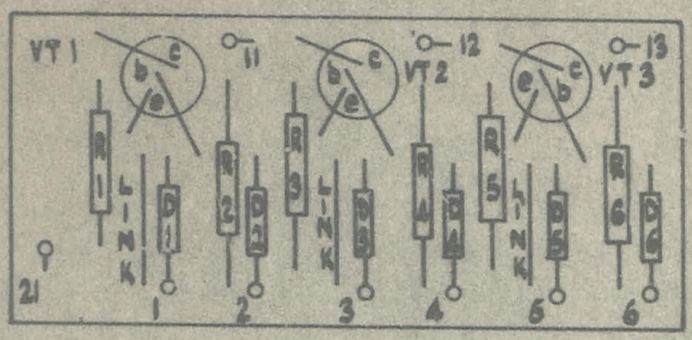


+6V ——— 21
0V ——— 23
-6V ——— 22

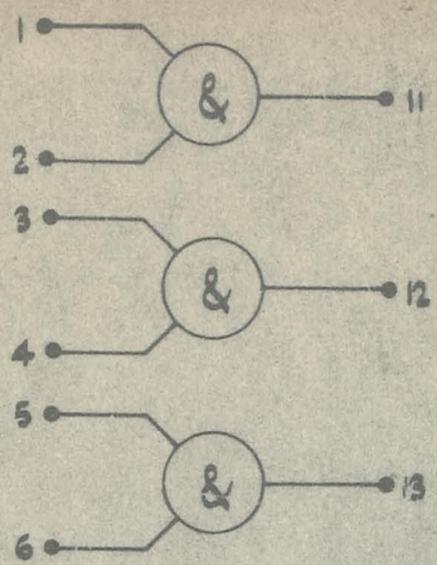
DRAWN C.A.C.	ISSUE No. 1 2										
CHECKED CS 456	A.R. No 1374 1505										
APPROVED ERM 6/5/66	DATE 26-4-66 29-6-66										
DATE	INITIALS C.A.C. R.W.C										

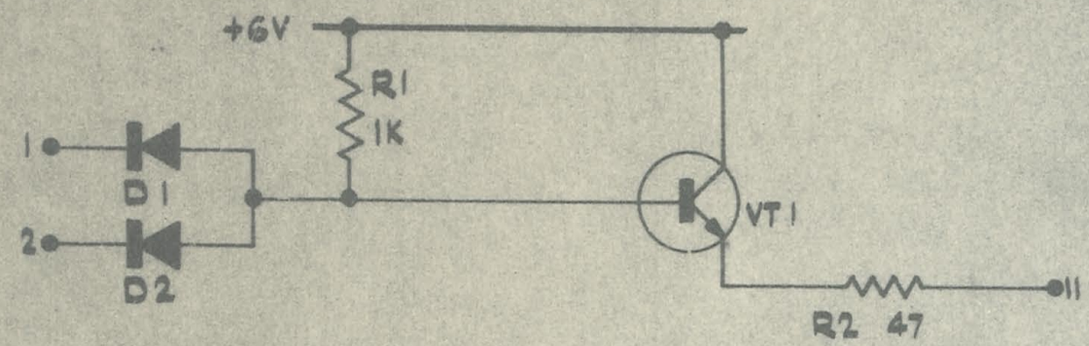
ELLIOTT BROTHERS (LONDON) LTD.

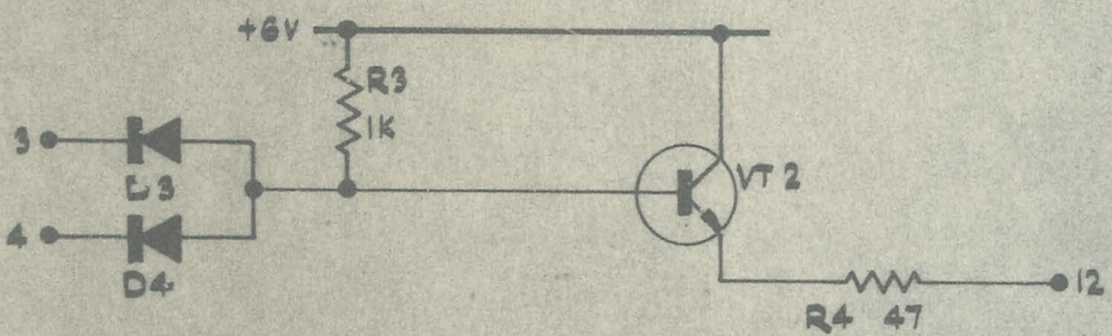
TITLE	INSTRUCTION SHEET
L.S.A. 21. DELAY.	322A7191 SHEET No 24 OF

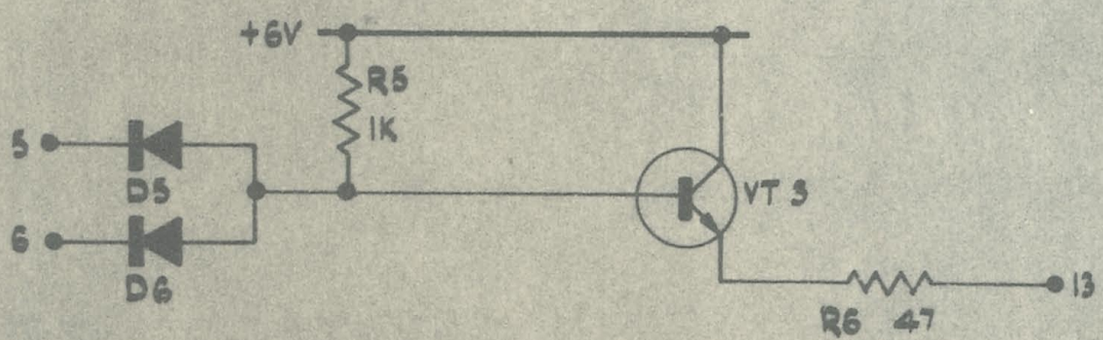


O/P'S 11, 12, 13, TO 50 Ω COAX.









DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100

+6V ——● 21

DRAWN C.A.C.	ISSUE No. 1									
CHECKED CS 456	A.R. No 1374									
APPR'VED	DATE 26-4-66									
DATE 16/5/66	INITIALS C.A.C.									

ELLIOTT BROTHERS (LONDON) LTD.

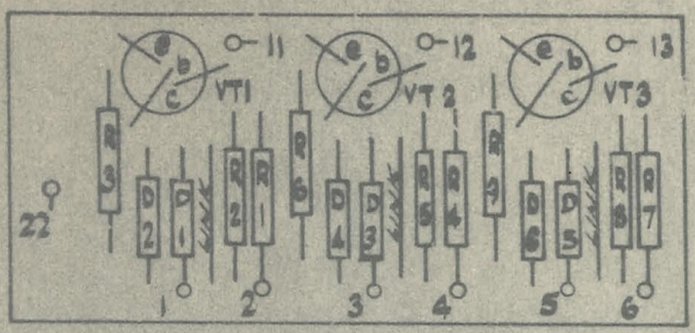
TITLE

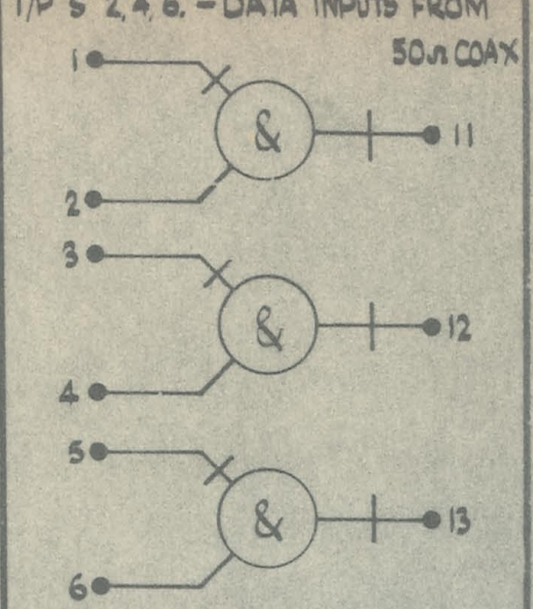
L.S.A. 22.
TWO INPUT TRANSMITTERS.

INSTRUCTION SHEET

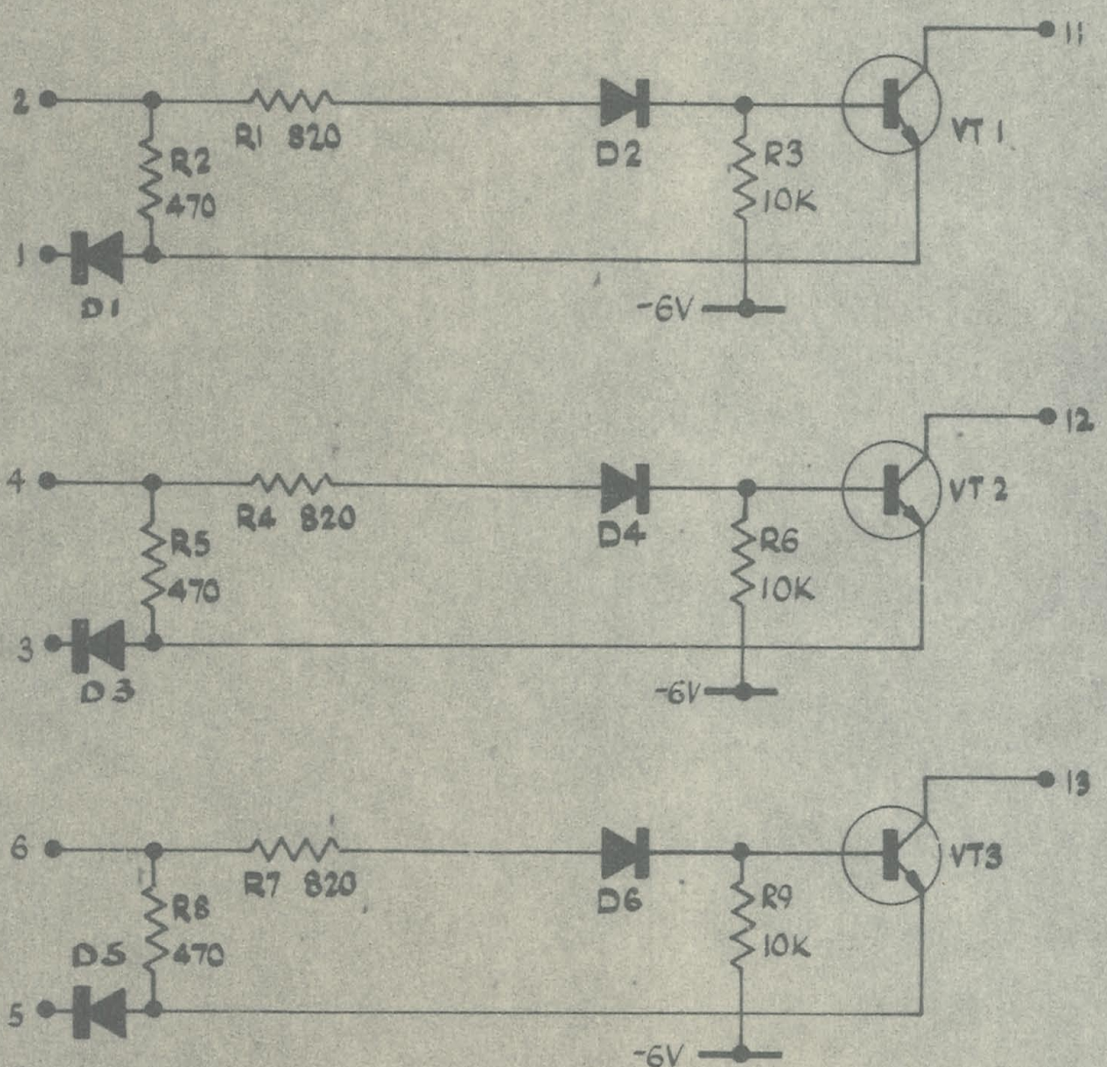
322 A 7191

SHEET No. 25 OF





I/P'S 1, 3, 5. CONNECTED TO AN O/P OF AN LSA 28.



DIODES ARE PURCH 101

TRANSISTORS ARE PURCH 100

-6V —— 22

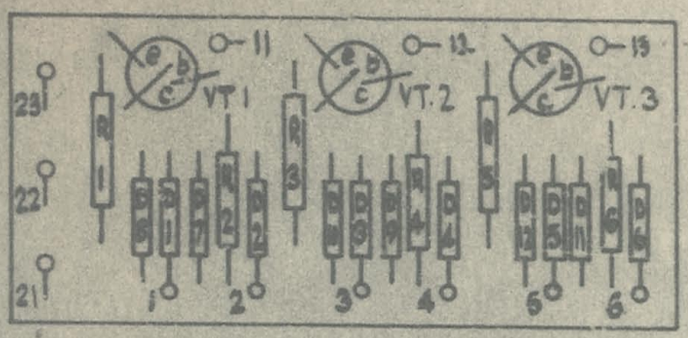
DRAWN C.A.C.	ISSUE No 1	2
CHECKED CS 456	A.R. No 1374	1796
ISSUED 2 RM 6.5.66	DATE 26-4-66	26/11/66
	INITIALS C.A.C.	

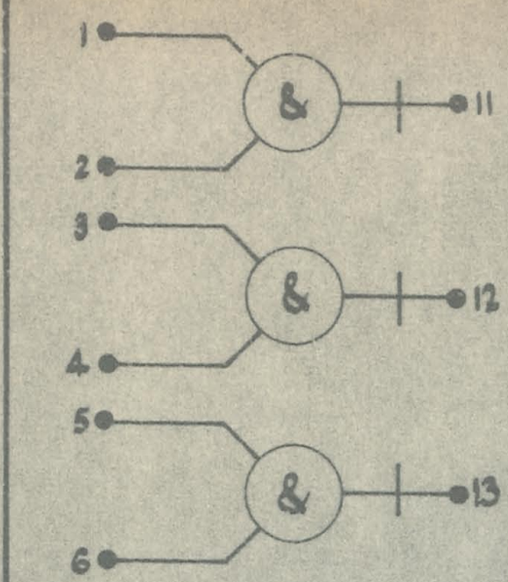
ELLIOTT BROTHERS (LONDON) LTD.

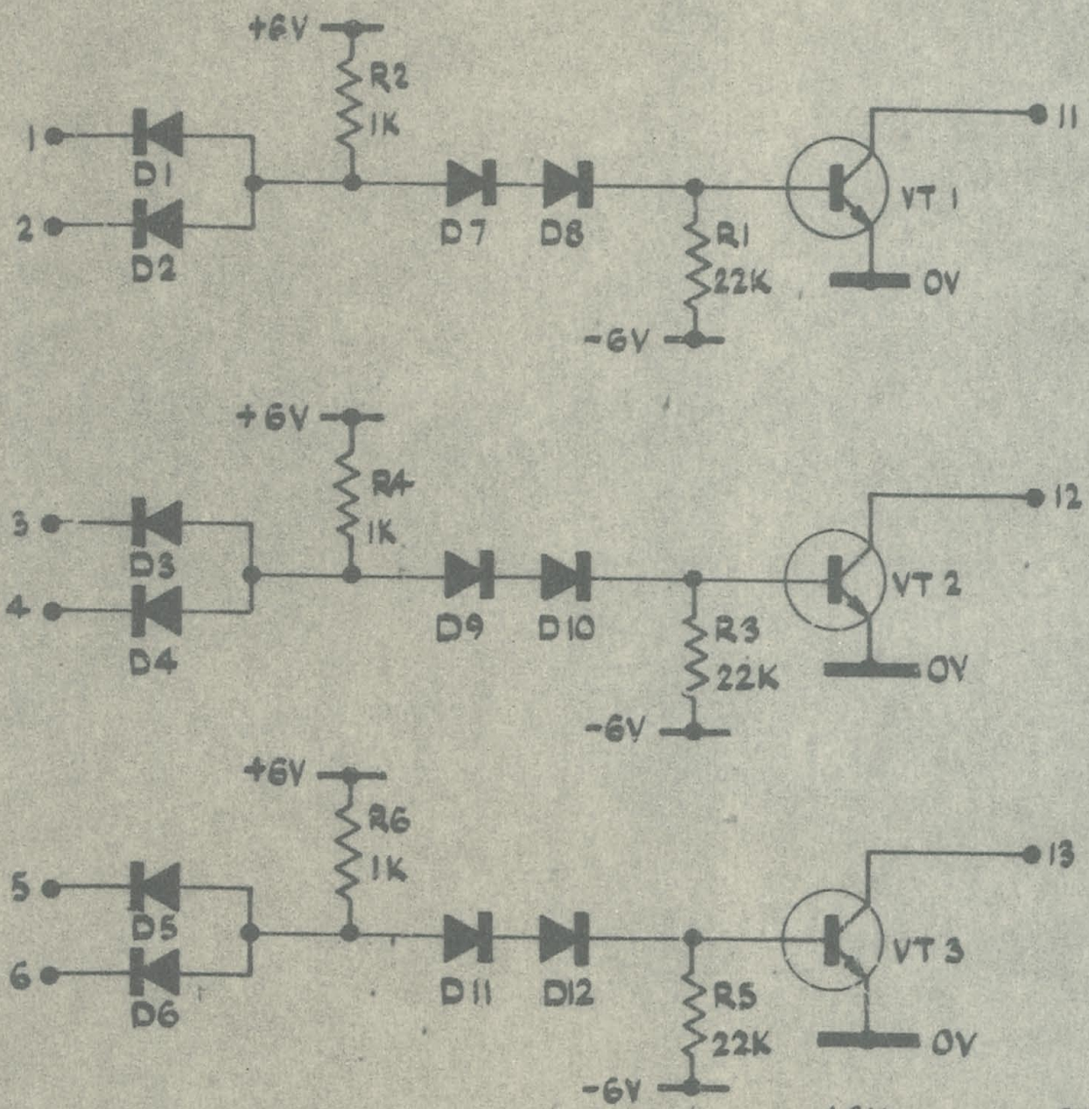
L.S.A. 23
GATED RECEIVERS.

INSTRUCTION SHEET
322 A 7191

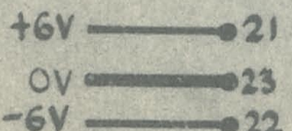
SHEET No 26 OF







DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100.



DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No	1374
APPROVED	[illegible]	DATE	26-4-66
DATE	12/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

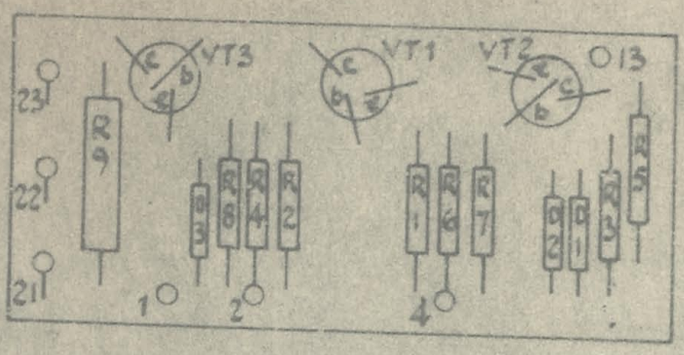
TITLE

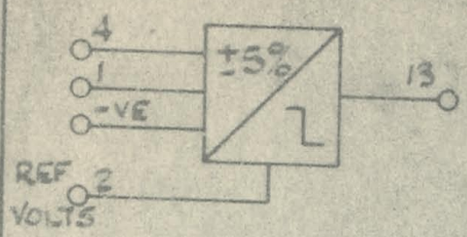
L.S.A. 28
2-INPUT NAND GATES.

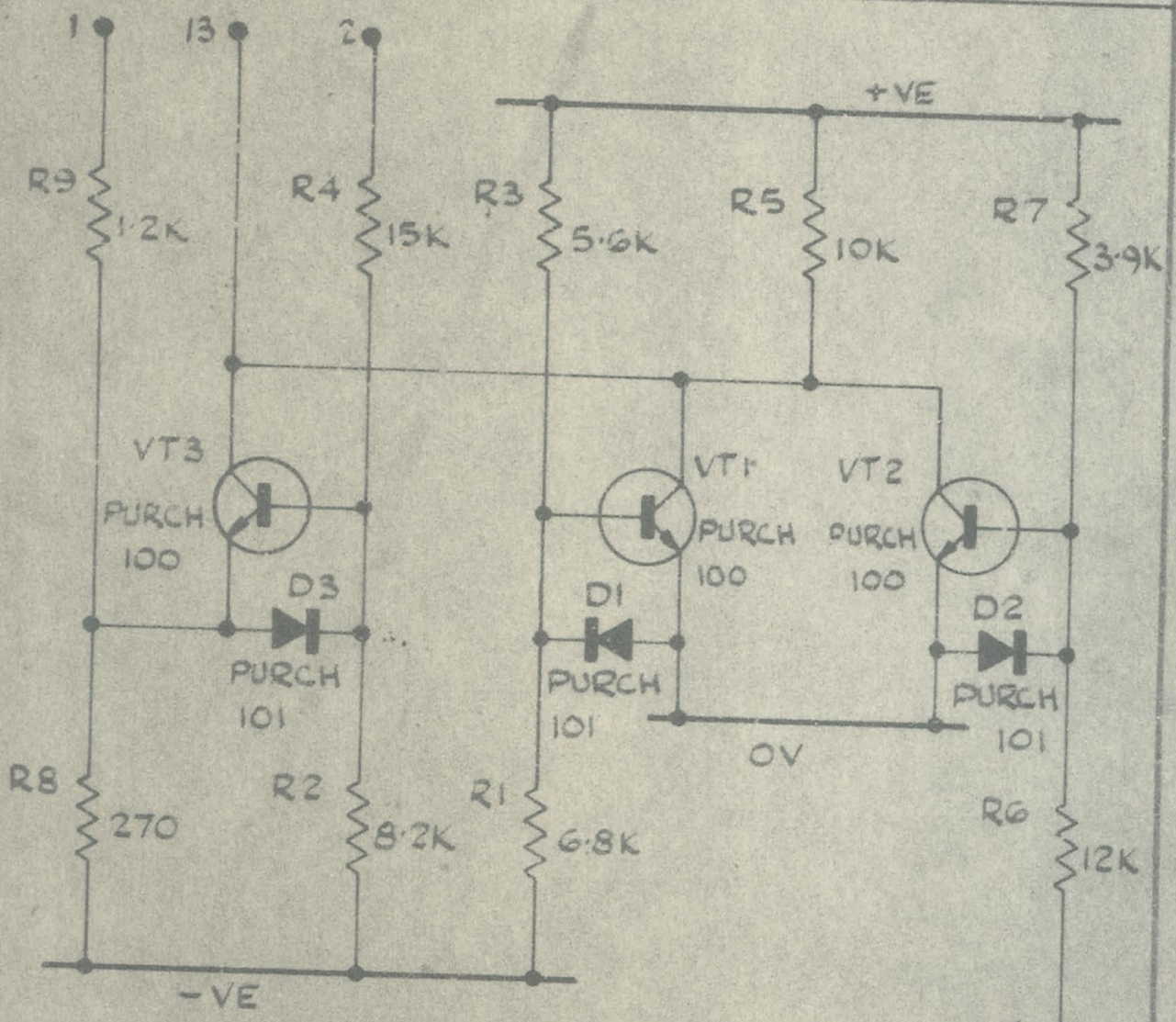
INSTRUCTION SHEET

322A7191

SHEET No. 27 OF







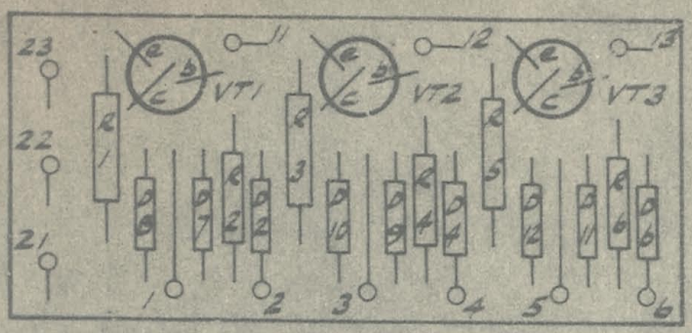
THE CHIEF ENGINEER MUST BE CONSULTED BEFORE THIS LSA IS USED ON ANY PROJECT OTHER THAN THE MARITIME STORE.

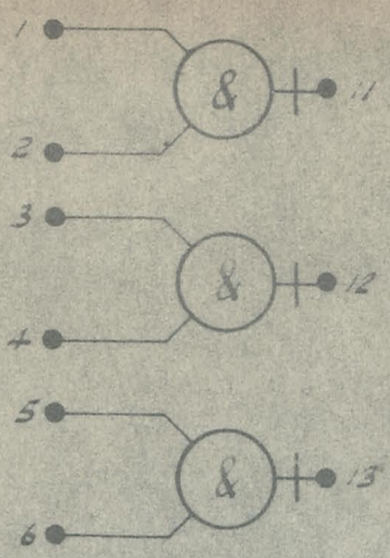
DRAWN KG.	ISSUE No. 1
CHECKED	A.R. No 1588
APPROVED	DATE 26·8·66
DATE	INITIALS KG

ELLIOTT BROTHERS (LONDON) LTD.

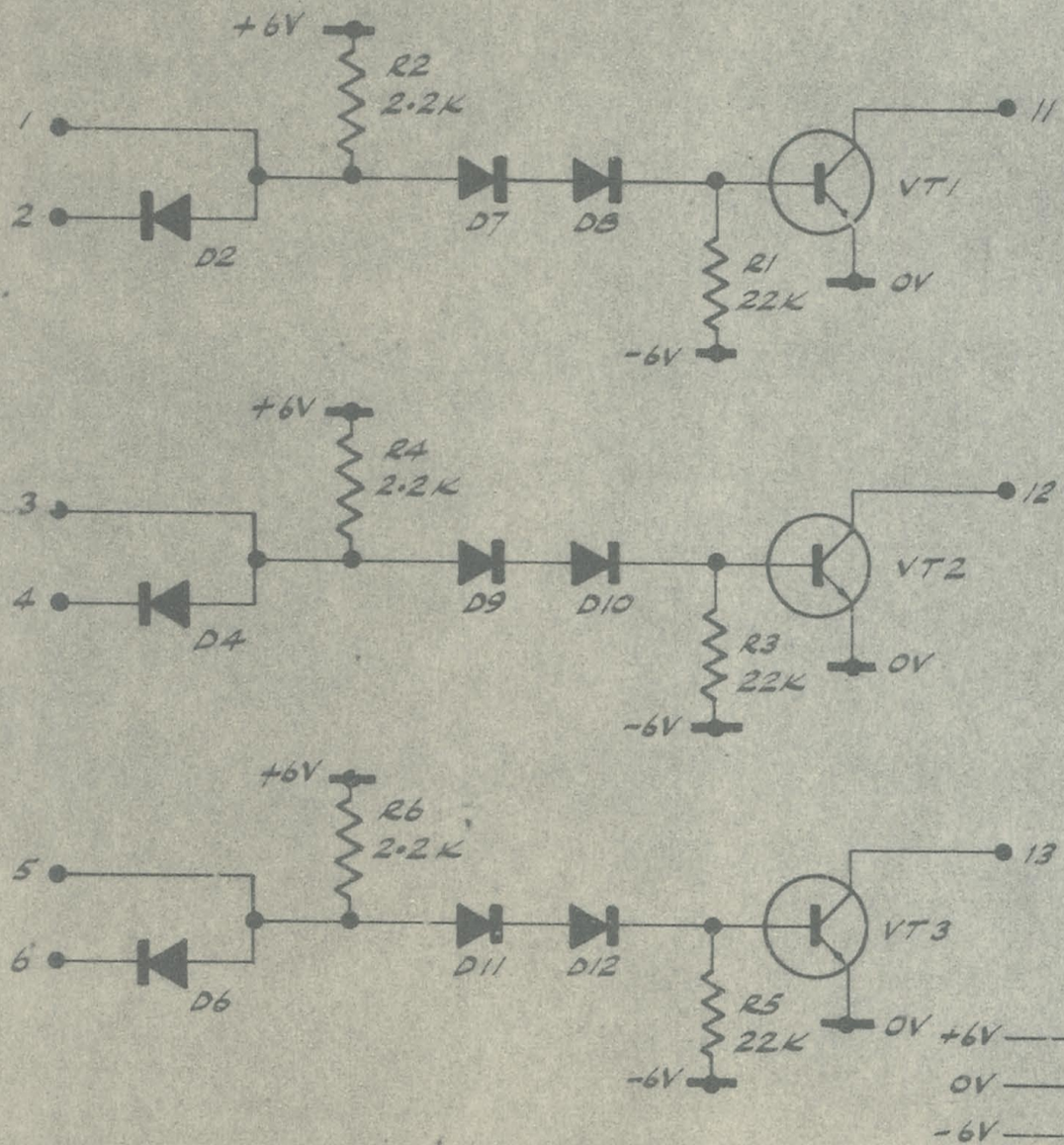
TITLE LSA 43 VOLTAGE RAIL SENSING	INSTRUCTION SHEET 322A 7191

SHEET No 28 OF





DIODES ARE PURCH-101
TRANSISTORS ARE PURCH-100



DRAWN N.G.R.H	ISSUE No 1	
TRACED C.S. 892 P.H.S.	A.R. No	
CHECKED	DATE 26.11.66	
	INITIALS A.H.	

ELLIOTT BROTHERS (LONDON) LTD.

LSA 44
2- INPUT NANDGATE 920B
(USED IN CONJUNCTION WITH LSA 23)

INSTRUCTION SHEET
322A7191

SHEET No 29
OF